Device Models for Silicon-on-Insulator (SOI) Insulated-Gate pn-Junction Devices for Electrostatic Discharge (ESD) Protection Circuit Design

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In this paper, SOI insulated-gate *pn*-junction devices (Lubistors [1]) are investigated as a source of SOI ESD protection circuits. Equivalent circuit models for circuit applications are presented. Device simulations of Lubistors are performed to assist the analysis of operation mechanisms of Lubistors in detail.

A schematic cross section of a SOI insulated-gate *pn*-junction device is shown in Fig. 1. Although the basic device structure is analogous to that of SOI MOSFETs, the device differs in having a lateral p^+-n-n^+ junction structure. There are three main regions: anode, channel, and cathode. The devices used in this study were fabricated on SOI wafers fabricated by the SIMOX technology [2]. The SOI layer thickness (t_s) was 80 nm, the gate oxide layer thickness (t_{ox}) 80 nm, and the buried oxide layer thickness (t_{BOX}) 380 nm. The gate width W_G was 50 μm and the gate length L_G was 10 μm. The doping concentration of body is $1x10^{15}$ cm^{-3}. Representative *I-V* characteristics of an actual device with L_G of 10 μm are shown by solid lines in Fig. 2. Non-saturation current characteristics appear under the condition of low gate voltages and high anode voltages.

From the simulation results [3], it is clear that the SOI insulated-gate *pn*-junction device has two operation modes, and that the modes can be freely switched by altering the gate and anode voltages. Fortunately, we have found that the characteristics described above can be reproduced by conventional device models for SPICE circuit simulation.

Two current components yielding the *I-V* characteristics are represented as the current flow components P1 and P2 in Fig. 3. In this configuration, the pMOSFET operates in the current saturation condition. The voltage source generates voltage kV_G, where k is the fitting parameter. The simulated *I-V* characteristics of the equivalent circuit model are shown by dotted lines in Fig 2 together with experimental results. Good agreement is achieved between experimental and simulation results.

It is reported that the ESD robustness of SOI technology is at only half that of conventional bulk-Si technology [4]. Therefore, a new ESD protection method that suits SOI technology is needed. S. Voldman et al. proposed an ESD protection method that uses SOI insulated-gate *pn*-junction devices (see Fig. 4) [5], where the ESD protection designs established for bulk-Si technology can be easily applied to SOI technology. However, they didn't provide design guidelines and details of protection behavior under ESD events.

In the present device simulations, the gate width of the SOI insulated-gate *pn*-junction device was 400 μm and the gate length was 0.5 μm. We can state that the SOI insulated-gate *pn*-junction device has the human-body model (HBM) immunity of about 15 V/μm and can handle currents of up to 10 mA/μm. A simple calculation shows that a device with a 400-μm gate width can sustain a 6 kV HBM pulse. This is twice the general HBM metric of 2 to 4 kV.

References

[1] Y. Omura, Appl. Phys. Lett. vol. **40**, pp. 528-529, 1982.
[2] K. Izumi, M. Doken, and H. Ariyoshi, Electron. Lett., vol. **14**, pp. 593-594, 1978.
[3] ISE Integrated Systems Engineering AG, "*DESSIS User's Manual* (release 7.0)".
[4] M. Chan, S. S. Yuen, Z.-J. Ma, K. Y. Hui, P. K. Ko, C. Hu, in Proceedings of IEEE Reliability Physics Symposium (San Jose, 1994) p. 292-298.
[5] S. Voldman, D. Hui, L. Warriner, D. Young, J. Howard, F. Assaderghi, and G. Shahidi, J. Electrostatics, vol. **49**, pp. 151-168, 2000.

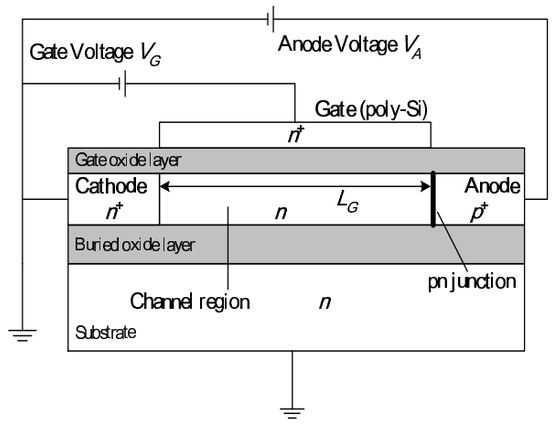

Fig. 1. Schematic cross section of an SOI insulated-gate pn-junction device

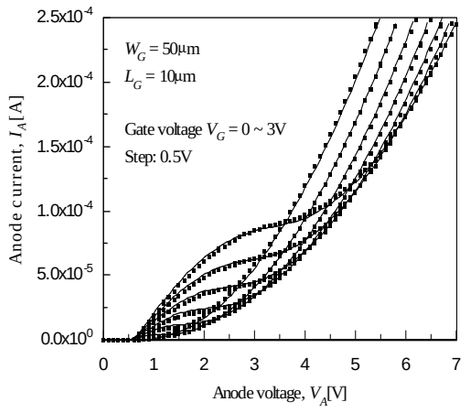

Fig. 2. Current vs. voltage characteristics obtained by the equivalent circuit model shown in Fig. 4. Solid lines are experimental results and dots are the simulation results of SPICE.

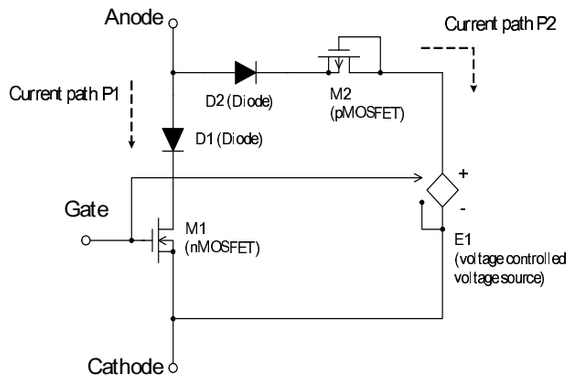

Fig. 3. Proposed equivalent circuit model of the SOI insulated-gate pn-junction device.

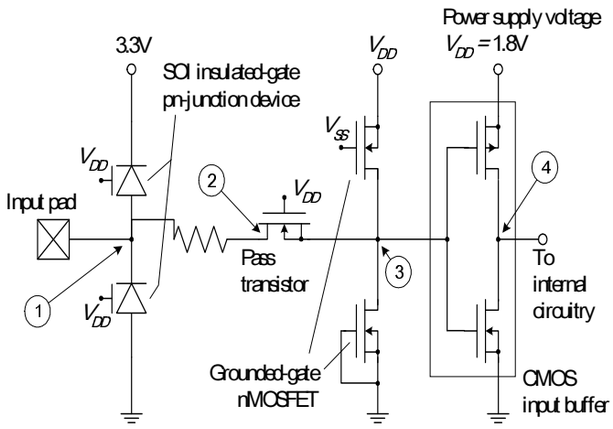

Fig. 4. SOI ESD protection circuit proposed by Voldman et al. The circled numbers indicate examined nodes.