Electron Mobility in strained-Si inversion layers grown on SiGe-on-insulator substrates

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Both strained-Si/SiGe inversion layers and Silicon-On-Insulator (SOI) devices have been proposed as promising candidates for improving the performance of Si CMOS technology[1][2]. However, the two semiconductor structures still suffer from severe limitations. One may wonder whether it could be possible to combine the two structures (strained silicon inversion layer and SOI inversion layers) to enjoy the advantages of each and at the same time, overcome the deficiencies they present separately. From the technology point of view, the answer is affirmative. Very recent studies have reported the feasibility of fabricating SiGe-based SOI substrates by separation-by-implanted oxygen techniques[3].Si/SiGe-OI (Figure 1) structures provide a good control of short channel effects (SCE), have a lower parasitic capacitance and higher radiation tolerance and, moreover, present mobility values that are much higher than those found in conventional SOI MOSFETs. Nevertheless, to achieve these results and at the same time provide a low off-state leakage current, allow operation at low voltages and avoid the floating body effect, the Si/SiGe structure sandwiched between the two oxides must be thin enough ($T_w=T_{Si}+T_{SiGe}<30$nm)[4], where T_{Si} and T_{SiGe} are the thicknesses of the strained-Si layer and of the relaxed SiGe layer, respectively. On the other hand, in order to keep the strain, the silicon layer must be sufficiently thinner than the SiGe layer. Therefore, taking into account both conditions, ($T_w<30$nm and $T_{Si}<T_{SiGe}$), the strained-silicon layer thickness has to be reduced to a very low value ($T_{Si}<10$nm). With such small values of T_{Si}, the extension of the electrons in these structures is less than in bulk devices, which could lead to an increase in the phonon scattering rate, and therefore to a mobility decrease. This could partially counteract the mobility increase achieved by the strain effects (lighter conduction effective mass and reduced intervalley scattering). It is therefore interesting to study the relative importance of this effect, i.e., to determine whether this phonon scattering rate increase is produced, and in the affirmative case, for which T_{Si} values, if any, this phonon scattering rate counteracts the mobility increase produced by the strain. To answer these questions we studied the electron transport properties in these strained Si/SiGe-OI structures by the Monte Carlo method. Poisson and Schroedinger equations are self-consistently solved to evaluate the carrier distribution in this structure. A Monte Carlo simulator is used to solve the Bolztmann transport equation.

We show that the electron mobility is greatly improved in strained Si/SiGe-OI devices, in comparison with unstrained SOI devices. In addition, when we put these strained-SOI devices side by side with strained silicon devices, the degradation in the electron mobility due to the electron confinement caused by the presence of the buried oxide is weak (10 %) if $T_w>10$nm. Therefore, we conclude that strained-Si/SiGe-on-Insulator inversion layers efficiently combine the improved mobility and velocity overshoot of strained-Si/SiGe devices with the advantages offered by SOI devices. However, we also show the important role played by the strained silicon layer thickness on electron mobility.

References:
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[4] T.Mizuno et al, IEDM-1999, p134, Dec.1999
[5] F.Gamiz et al., IEEE Trans.Electr. Dev. 45, p.1122 (1998)

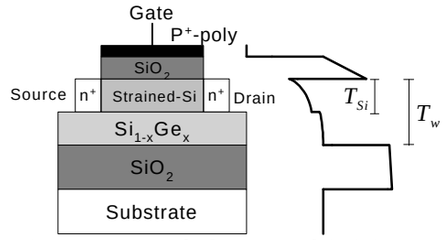

Fig. 1. Cross section of the strained-Si/SiGe-on-Insulator inversion layer under study.

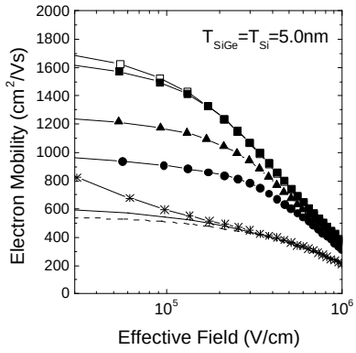

Fig.2. Electron mobility curves versus the transverse effective field for the simulated structure: circles: x=0.1; triangles: x=0.15; squares: x=0.3 ($T_{Si}=T_{SiGe}=5$nm). Mobility curves for unstrained SOI inversion layers: dashed line: $T_{Si}=T_w=5$nm; solid line: $T_{Si}=T_w=10$nm. The mobility curve corresponding to a bulk strained-Si/SiGe inversion layer with $T_{Si}=5$nm, and x=0.3. is represented by open squares. A mobility curve for a conventional bulk-silicon inversion layer is shown in asterisks.

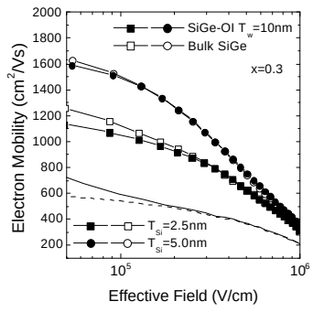

Fig. 3. (closed symbols) Electron mobility curves versus the transverse effective field for strained Si/SiGe-OI inversion layers(open symbols).Strained Si/SiGe bulk inversion layers (x=0.3) (without symbols) Conventional SOI inversion layers.

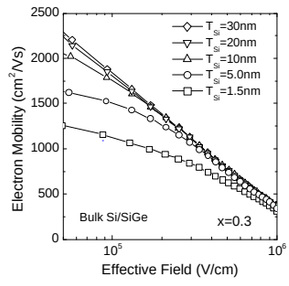

Fig. 4. Electron mobility curves versus the transverse effective field for strained Si/SiGe bulk inversion layers at room temperature for different values of T_{Si}. (x=0.3)