Accurate and Efficient Method for Accelerated History Effect Simulations

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INTRODUCTION

As Partially-Depleted (PD) SOI technology becomes very attractive for ULSI CMOS, accurate characterization of Floating-Body (FB) effects is needed for circuit design. In particular, very fast methods are required for history effect characterization (i.e. propagation delay dependence versus time (1)) of standard library cells. The 1st/2nd switch characterization gives bounds for propagation delays (2,3), but these values are generally not the real worst and best cases. In this study, we present for the first time a method that allows to know the whole history of a circuit (i.e. not only 1st switch, 2nd switch and steady-state propagation delays, but also worst and best cases) in a few minutes, whereas several days would be required by exhaustive simulations. This method can be easily implemented in industrial library characterization tools.

DESCRIPTION OF THE METHOD

The basic idea of the method is that floating-body potential variations can be linearized on large amounts of pulses. During one period of the input signal, the body potential variation of each FB transistor is evaluated. During the next period, a current is injected into the bodies from external sources until their potential variation reaches n times the calculated single pulse variation. Thus, the circuit sees the equivalent of 1+n pulses in 2 simulated periods, leading to an acceleration factor of (1+n)/2. This method is self-convergent because the single pulse body potential variation is null at the steady-state.
The implementation of this method simply consists in replacing each FB transistor by a sub-circuit containing the MOSFET, three voltage controlled voltage sources and one voltage controlled current source.

RESULTS

Simulations have been performed with BSIMPD V2.2.2 model in ELDO 5.6 simulator (4). The typical input signal used in this study has a period of 10ns and rise/fall times of 100ps. It should be noticed that the presented method is valid whatever the input signal, circuit, model and simulator used. Figure 1 shows the propagation delay evolution of the up input transition versus the re-calculated equivalent pulse number obtained on a single inverter, with L=0.13µm, Wn/Wp=0.5/1µm and a loading capacitance of 5fF. The reference curve is a standard simulation performed on 400,000 pulses. The accelerating method has been used with acceleration factor values of 10 over 40,000 pulses, 100 over 4,000 pulses and 1,000 over 400 pulses. The Acc=max case corresponds to an acceleration factor of 1,000 over 40 pulses (until the NMOS has reached its steady-state) and an acceleration factor of 10,000 (for the PMOS) over the 40 following pulses. We notice that identical worst/best cases are obtained with the exhaustive and accelerated simulations. Thus, the complete history of the gate is accurately simulated with only 80 pulses.
This method has also been applied successfully to the NAND family and to inverters chains. In the case of a two-inputs NAND presented figure 2, the steady-state has not been reached with the 400,000 pulses reference simulation (~16h) whereas the equivalent of 49 millions of pulses has been simulated with the accelerating method in less than 3 minutes (160 simulated pulses).

CONCLUSION

This study describes a powerful and accurate method for history effect simulations, that allows gains in CPU time higher than 1,000 in inverters chain simulations and up to 40,000 in NAND cases. It is shown that the whole history of a circuit can be obtained very accurately in a few minutes (a few tens of pulses), whereas several hours or days can be required by exhaustive simulations. Thus, this method allows to fully characterize a library (including worst/best cases) and to perform in-depth studies of history effects in reasonable simulation times.

REFERENCES

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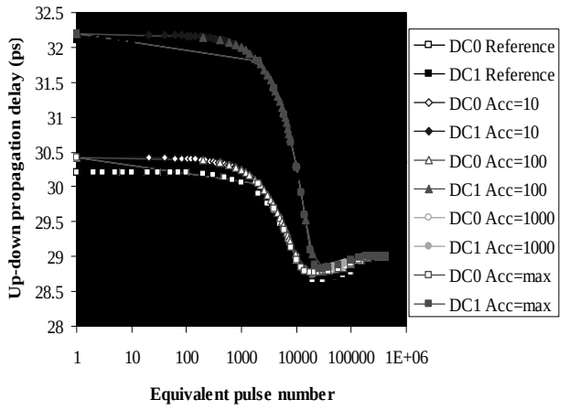

Fig. 1. *Propagation delay of an up transition of the input signal through a single inverter versus the equivalent pulse number for various acceleration factors.*

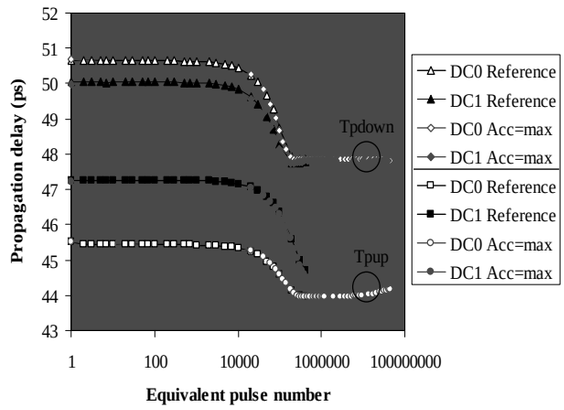

Fig. 2. *Comparison between the propagation delays extracted on a NAND for the reference and the accelerated simulations. Steady-state is not reached in the reference case.*