

Microscopic Theory of Nanoscale SOI MOSFETs

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We have carried out numerical modeling of sub-10-nm dual-gate SOI MOSFETs with ultra-thin, intrinsic (undoped) channel connecting bulk, n^+ -doped source and drain (Fig. 1). Such device is a close approximation to what may be called the “ultimate MOSFET”, but still allows practical implementation using either planar, or fin-type, or vertical geometry – see, e.g., recent reviews [1-3].

The model shown in Fig. 1 was studied earlier using the WKB approximation [4, 5]. However, as the gate length L is scaled below ~ 10 nm, this approximation becomes inadequate for the description of electron transport, in particular of the source-to-drain tunneling under the gate-controlled potential hump in the channel. (Such tunneling, together with the loss of electrostatic control, are two main sources of device degradation at $L \rightarrow 0$ [3-5].) The goal of this work was the modeling of such nanoscale devices using the numerical solution of the Schrödinger equation for electrons in the channel.

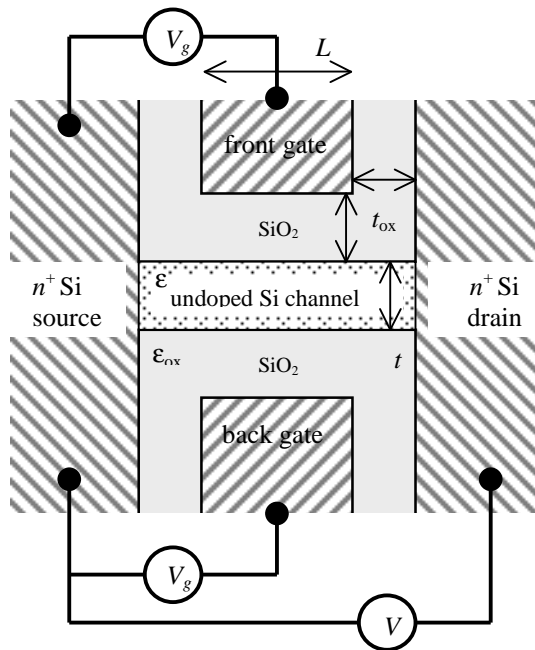


Figure 1. The model of a double-gate SOI MOSFET with ultrathin undoped channel, accepted in this work.

Earlier work [4, 5] has shown that in order to reach high performance, both gate oxide (t_{ox}) and channel (t) have to be of the order of, or below then 2 nm, i.e., considerably smaller than L . As a result, a reasonably good description of the device properties may be achieved using a self-consistent solution of the 1D Schrödinger equation and 2D Poisson equation. (The account of the electric charge of carriers not only in the classically allowed regions, but also under the tunnel barrier, is important [5].)

Moreover, estimates show that if the recent success in fabrication of 5-nm-thick SOI channels with high mobility [6] is extended to channels twice thinner, electron scattering inside the channel will have small effect on electron propagation, and may be neglected. These approximations allow a reasonably fast calculation of all transistor characteristics on modern workstations.

Our preliminary results show that room-temperature devices with gate length as short as 5 nm still have high transconductance and relatively small DIBL effects, and thus may be suitable for nearly all digital applications. Moreover, transistors with L as small as 3 nm may still feature voltage gain above unity, and hence may be the basis for digital electronics.

However, all characteristics of such devices are extremely sensitive to very small variations of their geometrical parameters (L , t , and t_{ox}), as well as single charged impurities inside (or in the immediate vicinity of the channel). As a result of this sensitivity, fabrication of sub-10-nm devices with acceptable yield would require extremely tight specifications, far exceeding recent ITRS projections for the Year 2016 [7].

In our report, we will present the calculated source-drain I - V curves of nanoscale MOSFETs, their subthreshold characteristics, and voltage gain vs. gate voltage curves for various parameters of the transistors, and the results of analysis of parameter sensitivity of these devices. Possible ways to decrease this sensitivity will be also discussed.

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