Comparison of partially and fully depleted SOI transistors down to the sub 50nm gate length regime

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Introduction

Whereas SOI transistors are in general considered as attractive devices for the future CMOS technology nodes, there is still an ongoing discussion about the benefits and difficulties associated with fully depleted (FD) and partially depleted (PD) concepts. This work reports on an extensive comparison of these two transistor types. The devices were fabricated with gate lengths as small as 25nm under identical conditions apart from the channel doping. Characteristic strengths and shortcomings of these concepts will be discussed.

Processing

The devices were fabricated on ELTRAN SOI wafers with a silicon thickness of 45nm and a buried oxide of 100nm. A process flow with special SOI process steps such as an advanced MESA isolation was employed. The oxide under the n^+-poly-Si gate had a thickness of 3nm. The gates were defined by electron beam lithography. The transfer of these patterns was performed with an optimized etching process. A typical transistor structure with 28nm gate length is shown in Fig.1. For the n-channel devices considered here, both transistors with 'undoped' ($1 \cdot 10^{16}cm^{-3}$) and doped ($9 \cdot 10^{17}cm^{-3}$) channels were fabricated. The width of the analyzed devices was 0.4µm.

Device Characteristics

The output characteristics of transistors with 200nm gate length are shown in Fig.2a, parameter is the gate overdrive voltage. A clear kink effect is observed with channel doping, indicating the floating body effect of a PD device. In contrast, the undoped channel device shows the characteristics of a FD device. In addition, the on-current of the latter is about 30% higher due to better mobility.

While these results are in favor of FD, the DIBL, see transfer characteristics in Fig.2c-f, and the scaling behavior of this device are worse. As can be seen in Fig.2b, $V_{th}(L)$ is nearly constant for PD devices in the range of 50 – 200nm, whereas FD shows a rolloff of 0.6V. The better channel control of the PD device can also be recognized in the transfer characteristics of the 50nm devices. At V_{DS} = 1V it can be turned off down to 10^{-12}A/µm, unlike the FD device. On the other hand, the measurements clearly reveal the potential of nearly ideal subthreshold slope S in FD devices, Fig.2g,h. S < kT·ln10 for higher V_{DS} occurs for PD due to the floating body effect and avalanche multiplication.

This is consistent with simulations where a ratio L_G/T_{Si}>=4:1 is required for good off current behaviour of FD devices. In order to fully exploit the benefits of FD devices, ultra-thin Si-layers are needed in the sub 100nm regime. For the PD devices, however, this high ratio is not required, characteristics like subthreshold slope and DIBL do not change significantly over a wide range of gate length, before at 50nm gate length the device performance begins to degrade. Drift-diffusion simulations have been carried out to verify the results and will be presented in the full paper.

Conclusion

Our results reveal that the SOI thickness T_{Si} limits the scaling potential of FD to about $4 \cdot T_{Si}$. These FD devices show superior performance compared to the corresponding PD devices. For shorter gate lengths PD devices offer the advantage of relaxed requirements on the silicon thickness with improved subthreshold behavior at the cost of lower on-currents.

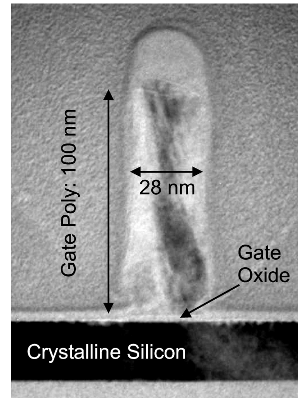

Fig.1: *TEM micrograph of SOI transistor with 28nm gate length after etching. (The silicon thickness is 27nm in this case.)*

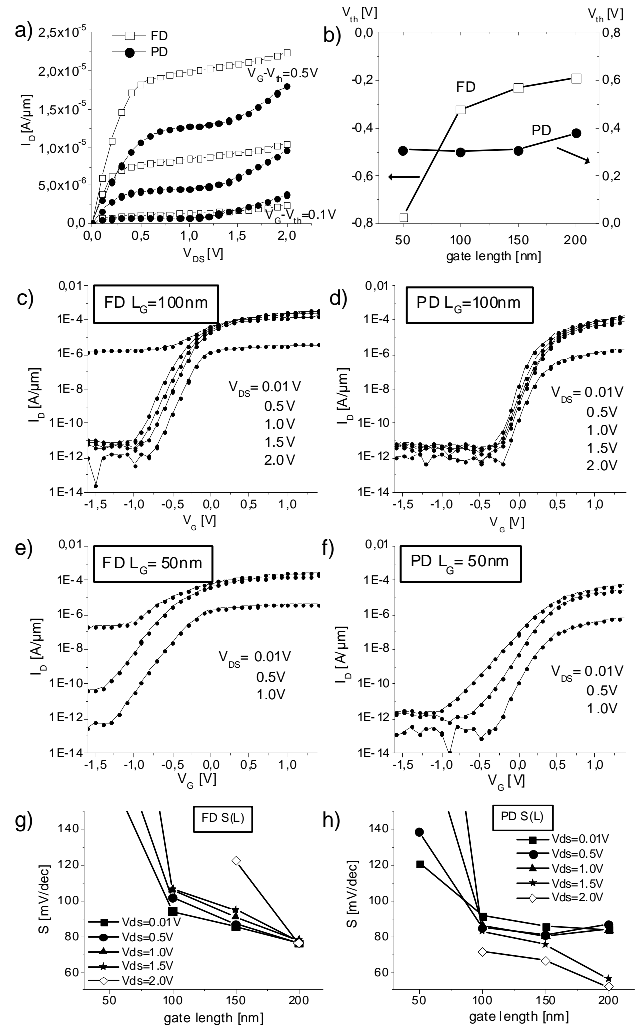

Fig.2: *a) Output characteristics of SOI devices with L_G=200nm, undoped and doped channels (open vs. full symbols) b) Comparison of V_{th} rolloff for FD and PD devices c-f) Transfer characteristics for L_G=100nm (c,d) and L=50nm (e,f) g,h) Subthreshold slope vs. gate length. The figures (c,e,g) refer to FD, (d,f,h) to PD devices.*