Saturation Current Model for the N-channel G^4-FET

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Abstract — A new saturation current model is presented for the n-channel G^4-FET, a novel 4-gate transistor [1-2]. The model is verified against measurement results from G^4-FETs fabricated using a commercially available 0.35-micron partially-depleted SOI process. A 3-dimensional illustration of the G^4-FET is shown in *Figure 1*. Since the G^4-FET is an accumulation-mode device, the conventional first-order JFET model [3] provides the basis for the G^4-FET saturation current model. The JFET model's gate-to-source voltage is replaced by V_{JG}, the bias voltage applied to the G^4-FET's junction (or lateral) gates. Then, to include the additional gate bias effects exhibited by the G^4-FET's saturation I-V characteristics, the new model develops hierarchical equations for the JFET zero-bias saturation current parameter, I_{DO}, and the pinch-off voltage, V_P.

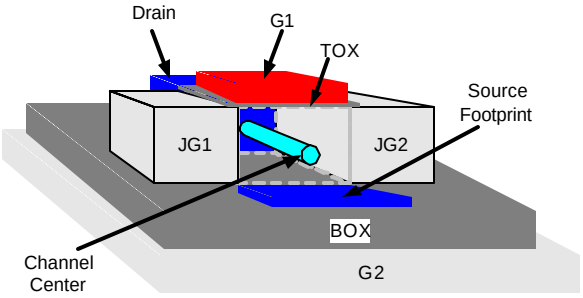

Figure 1. 3-dimensional illustration of the G^4-FET.

Parameter values for the new model were extracted using curve-fitting techniques. A plot of simulation (using the new model with extracted parameter values) versus measured I-V characteristics for a 0.4µm/0.9µm n-channel G^4-FET is provided in *Figure 2* for five different top-gate (V_{G1}) bias conditions. The new model achieves very good accuracy for top-gate bias conditions ranging from depletion to weak accumulation. These and other systematic experiments confirm the model. A complete description of the model, along with verification, will be provided in the full paper.

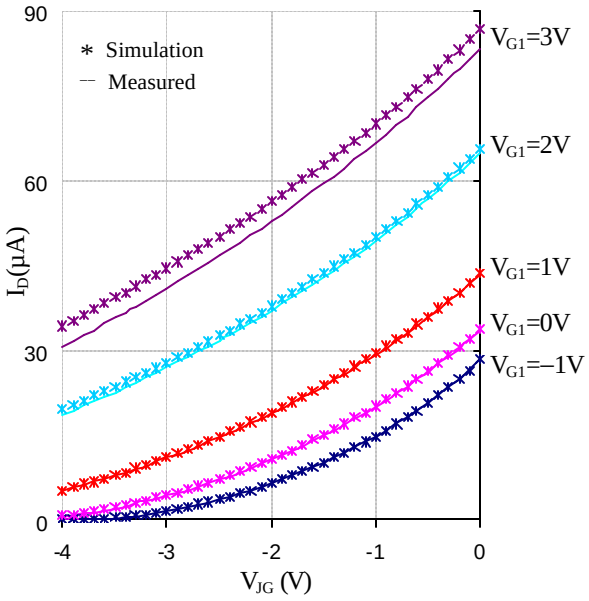

Figure2. I_D vs. V_{JG} curves for measured and simulated 0.4µm/0.9µm n-channel G^4-FET (V_{DS}=4.0V).

References

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