SOI Thermal Resistance and Its Application to Thermal Modeling of SOI MOSFETs

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Traditionally, SOI *channel* thermal resistance R_{thc} is used to describe heat loss in SOI devices to *BOX* [1-4]. R_{thc} was proposed to be [3]

$$R_{thc} = \sqrt{t_{box} / (k_{ox,eff}\, k_d\, t_{Si})} \Big/ (2w) , \qquad (1)$$

where w, t_{box}, t_{Si}, k_d and $k_{ox,eff}$ are device width, buried oxide thickness, *Si* film thickness, and effective drain/source and oxide thermal conductivities, respectively. This is however only valid for a drain/source region much longer than its thermal length and may not be realistic. In this study, *Si* film thermal resistance defined as $R_{thf} = \langle T_{Si}\rangle/(I_d V_{ds})$ is proposed for study of heat flow in SOI devices. Based on heat flow from the channel to the source/drain and to *BOX* and *FOX*, a R_{thc}-R_{thf} relation is derived from the heat flow equation,

$$\frac{1}{R_{thc}} = \frac{k_{ox,eff,c}\, L_g\, w}{t_{box}} + \frac{2wk_d\, t_{Si}}{\lambda_d \sinh\frac{L_d}{\lambda_d}} \left[\cosh\frac{L_d}{\lambda_d} - \left(\cosh\frac{L_d}{\lambda_d} + \frac{2k_{ox}\lambda_d \sinh\frac{L_d}{\lambda_d}}{k_d\,(t_{box}+t_{Si})} \sum_{m=1,3,5...}^{\infty} \frac{\sin\alpha_m t_{box}}{\alpha_m t_{box}} \sin\alpha_m (t_{box}+\frac{t_{Si}}{2}) \right)^{-1} \right], \qquad (2)$$

where L_g is the gate length, L_{Si} is the *Si* island length, $\alpha_m = m\pi/2/(t_{box}+t_{si})$, thermal length in the drain/source is give as $\lambda_d = \sqrt{R_{thf}\, w t_{Si} k_d L_{Si}}$, and $k_{ox,eff,c}$ is extracted from a curve-fitting equation for the stripline capacitor [6] based on the electrostatics and thermostatics analogy $L_g/t_{box} < 0.7$

$$k_{ox,eff,c} = k_{ox} [1 + 0.882 \frac{t_{box}}{L_g} - \frac{2t_{box}}{L_g} (0.35 - \frac{L_g}{2t_{box}})^2] .$$

For $L_d >> \lambda_d$, Eq. (2) reduces to Eq. (1) if $R_{thf} = t_{box}/(k_{ox,eff} L_{Si}\, w)$. $k_{ox,eff}$ and $k_{ox,eff,c}$ are effective oxide conductivities for the *Si* film and the channel respectively. The former has finite *Si* film thickness, and the latter is only for a thin plate at the bottom of the channel. Fig. 1(a) shows that the maximum deviation of Eq. (2) is below 6% for 40nm≤ t_{Si} ≤400nm. With measured R_{thco} [4,5], R_{thfo} can be estimated from Fig. 1(a).

R_{thf} describing heat loss to the oxide/substrate is applied to develop an analytical heat flow model in SOI devices. Heat loss to poly or interconnect lines is modeled by thermal resistance of the interconnect or poly line, $R_{int,n}$, where the subscript n denotes the s (source), c (channel) or d (drain) region. This is only valid for physical line length shorter than its thermal length. The thermal length is estimated to be near 6-13μm or 2-3μm for the *M1* or poly line, respectively [1,3].

Fig. 1(b) displays the temperature profiles in an SOI device with t_{Si}=150nm. For simplicity, $R_{int,s}=R_{int,c}=R_{int,d}$. Comparison between the analytical model and device simulation indicates that the analytical model provides a very good description for heat flow in SOI devices. Due to self-heating and the thin *Si* island, large temperature variation is observed in the *Si* film, and the peak temperature is considerably greater than the average channel temperature. These are useful information for study of electronic characteristics and device reliability.

The developed model is extended to describe heat flow in a 2-device SOI structure shown in Fig. 2. In the simulation, $T_{int,Is}$=20K, $T_{int,Ic}=T_{int,IIc}$=10K, and 3 values of temperature for $T_{int,IId}$ (20K, 40K and 80K) are applied. Fig. 3(a) shows that the increase in $T_{int,IId}$ raises temperatures in Devices I and II. In Fig. 3(b), the simulation is carried out without the interconnect between Devices I and II; i.e., heat exchange between these 2 devices can only go through *FOX*. Without heat flow through the metal line between devices, the temperature profile in Device I is nearly unchanged, when $T_{int,IId}$ changes from 20K to 80K regardless of the substantial temperature increase in Device II. Results clearly suggest that heat exchange between devices in SOI structures through oxide is negligible. This demonstrates the importance of the interconnects for heat exchange between devices and for cooling in the SOI structures.

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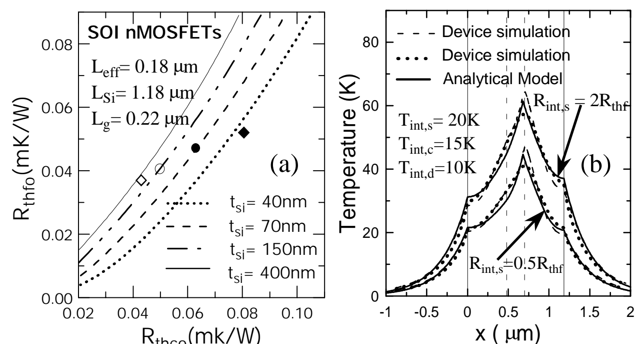

Fig. 1 (a) R_{thfo} vs. R_{thco}. $R_{thco}=wR_{thc}$, and $R_{thfo}=wR_{thf}$. Symbols are from the device simulation. (b) Temperature along the channel direction. Dash and dot lines are results at the top and bottom of the *Si* film, respectively. Curves extend to *FOX* for $x < 0$ and $x >$ 1.18μm

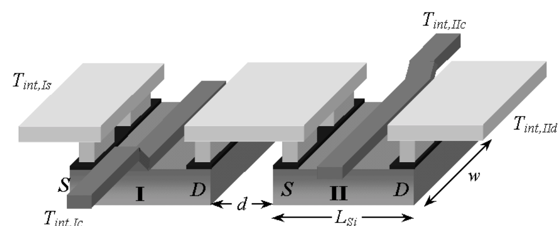

Fig. 2 Simplified 2-device SOI structure. 0.9mW/μm is applied to each device. The Device-I drain and Device-II source are interconnected by aluminum vias and an *M1* line. $T_{int,Is}$, $T_{int,Ic}$, $T_{int,IIc}$ and $T_{int,IId}$ are temperatures at the end of interconnect or poly lines. Separation of 2 devices d = 0.2μm.

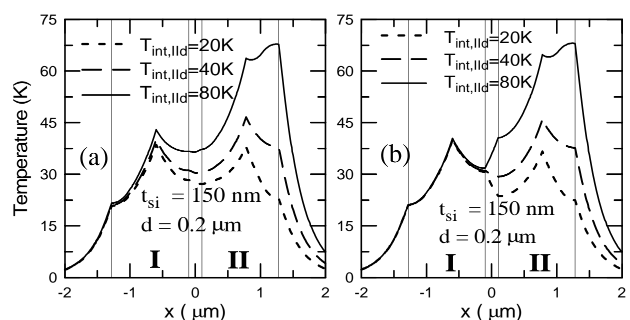

Fig. 3 Temperature profiles in the 2-device SOI structure (a) with and (b) without the interconnect between the devices.