Quasi-Three-Dimensional Device Simulation of Fully Depleted MOSFET/SOI Focused on Surface Roughness

Motoi Nakao, Hirofumi Iikawa, and Katsutoshi Izumi
RIAST, Osaka Prefecture University,
1-2, Gakuencho, Sakai, 599-8570, Japan

INTRODUCTION

Electron mobility in an inversion layer of MOSFET is one of the most important factors influencing a device performance. The relationship between the mobility and an effective normal field can be universally described using coulomb, phonon, and surface roughness scattering terms [1]. The scaling of a device in the future demands a higher performance in operation in a higher normal effective field caused by thinner gate oxide. Because the surface roughness scattering term is dominant in a high effective normal field, it becomes more important to reduce the surface roughness, especially in case of a fully depleted (FD) MOSFET/SOI with an ultrathin top Si layer. However, it has not yet been clearly verified how the surface roughness influences the device performance.

In this work, we propose a novel TCAD simulation method for an FD MOSFET/SOI. The simulation was performed quasi-three dimensionally (3D), focusing on a surface roughness.

EXPERIMENTAL

A SIMOX substrate with a thermal oxide was annealed in a hydrogen atmosphere at about 1400℃ to reduce a surface roughness. After the top SiO_2 layer was removed, the surface topography was measured using atomic force microscopy (AFM). Numerical topographical data of the central 100nm × 100nm (40 × 40 pixels) in the AFM image were used as a device structure for a TCAD simulation. An as-received SIMOX substrate, and a SIMOX substrate with a 10nm-thick thermally grown oxide, were also used as control samples.

SIMULATION

Simulations of FD MOSFETs/SOI device characteristics were performed using ISE-TCAD. Structural device parameters used for the simulations were: a gate oxide thickness of 2 nm, a top Si layer thickness of 10 nm, a buried oxide thickness of 50 nm, a gate length of 100 nm, and gate width of 100 nm.

Surface topographical data obtained from AFM were employed for a geometric interface structure between the gate oxide and the top Si layer (channel) in a MOSFET. As shown in Fig. 1, the top Si layer was divided into ten regions for the quasi-3D simulation. Each divided gate width was 10 nm, which is comparable to the De Broglie wavelength of Si. An AFM line profile of each region, which was averaged along the direction of a channel, was used for the TCAD simulation.

RESULTS AND DISCUSSION

Figure 2 shows simulated I_D–V_G characteristics of FD MOSFETs for the as-received SOI substrate. Ten curves correspond to ten regions with gate widths of 10 nm. Despite neighboring regions, each curve shows different characteristics for high V_G, *i.e.*, high normal effective field. This result indicates that even a slight difference in the surface roughness at the top Si layer influences the device characteristics.

Figure 3 shows the simulated I_D-V_G curves for as-received, oxidized, and hydrogen-annealed substrates. Each I_D sums up currents for ten devices with gate widths of 10 nm (seen in Fig. 1). The I_D of the hydrogen-annealed substrate is the largest in high normal effective field due to being the most effective decrement of surface roughness. The results indicate that that the proposed quasi-3D device simulation by TCAD using surface topographical data is effective for a detailed analysis of FD MOSFETs/SOI performance.

SUMMARY

A novel simulation method for FD MOSFET/SOI has been proposed. Quasi-3D simulations focusing on surface roughness were conducted by employing numerical topographical data from AFM measurement for graphical data in TCAD, and by dividing device structures in the proper dimensions along the channel direction. The results indicate not only the usefulness of the simulation, but also its effectiveness in analyzing the influence of surface roughness upon the device performance.

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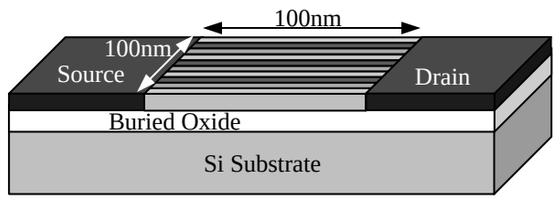

Figure 1. Divided structure for quasi-3D TCAD simulation.

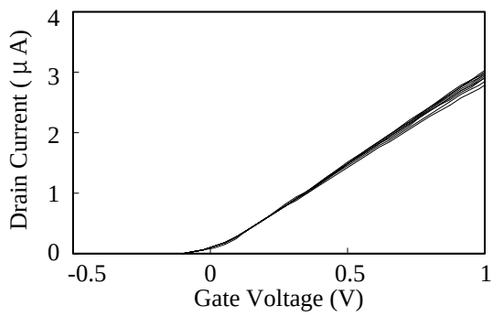

Figure 2. I_D-V_G curves from ten divided channel regions in as-received SOI.

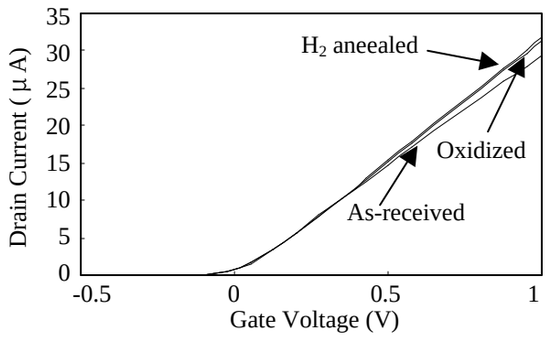

Figure 3. I_D-V_G curves for substrate with various surface roughnesses.