# An Accurate Model for Threshold Voltage and S-factor of Partially-Depleted Surrounding Gate Transistor(PD-SGT)

Y. Yamamoto, M. Hioki, R. Nishi, H. Sakuraba and F. Masuoka
Research Institute of Electrical Communication, Tohoku University
2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan

**Abstract.** This paper proposes an accurate model for threshold voltage and S-factor of partially-depleted surrounding gate transistor(PD-SGT) for the first time. Moreover, accurate electric field, potential and depleted region width peculiar to a cylindrical structure are obtained. The results numerically calculated by this model agree well with those of three-dimensional(3D) device simulator.

**Introduction.** In order to achieve future ULSI's, three-dimensional(3D) structured SGT[1] is proposed. Fabricated on a cylindrical pillar of silicon, SGT has the benefits of packing higher densities, reducing the short channel effects and improving the S-factor. Conventional analytical model of Bulk MOSFET can't be applied to the analysis of cylindrical structured SGT. Although fully-depleted SGT(FD-SGT) has been analyzed [2], threshold voltage and S-factor of PD-SGT have not been analyzed yet. This paper proposes an accurate model considering 3D cylindrical structure for threshold voltage and S-factor of PD-SGT.

**New Models for PD-SGT.** Fig.1(a) and (b) show bird's-eye view and cross-sectional view of Nch-PD-SGT. The SGT arranges source, gate and drain vertically. The gate electrode surrounds the silicon pillar. Silicon body is partially-depleted as shown in Fig.1(c). In deriving an accurate model, we consider a subthreshold region of the long-channel structure using a depletion approximation. In applying the Gauss's Law to the gate oxide region and integrating the result, the electric field $E_{ox}(r)$ and the potential $V_{ox}$ in the oxide region are obtained as follows

$$E_{ox}(r)=\frac{qN_aW_d(2R-W_d)}{2\varepsilon_{ox}\cdot r} \quad \text{for} \quad R<r<R+t_{ox} \qquad (1)$$

$$V_{ox}=V_{ox}(R,N_a,t_{ox},W_d)=\frac{qN_aW_d(2R-W_d)}{2\varepsilon_{ox}}\ln(1+\frac{t_{ox}}{R})$$

$$\text{for} \quad R<r<R+t_{ox} \qquad (2)$$

Similarly, the electric field $E_{si}(r)$ and the potential $\phi_s$ in the depleted region are obtained as follows

$$E_{si}(r)=\frac{qN_a}{2\varepsilon_s}\left\{r-\frac{(R-W_d)^2}{r}\right\} \quad \text{for} \quad R-W_d<r<R \qquad (3)$$

$$\phi_s=\phi_s(R,N_a,W_d)=\frac{qN_a}{2\varepsilon_s}\left\{\frac{W_d(2R-W_d)}{2}+(R-W_d)^2\ln(1-\frac{W_d}{R})\right\}$$

$$\text{for} \quad R-W_d<r<R \qquad (4)$$

where R is the silicon pillar radius, $N_a$ is the body impurity concentration, $t_{ox}$ is the gate oxide thickness, $W_d$ is the depleted region width under the gate, r is the distance from the center of silicon pillar, q is the charge of electron, $\varepsilon_{ox}$ is the dielectric constant of silicon dioxide and $\varepsilon_s$ is the dielectric constant of silicon. We assume the electric field and the potential in the non-depleted region ($0<r<R-W_d$) of silicon pillar to be zero. The relationship between the gate voltage $V_g$, (2) and (4) is given by

$$V_g-V_{fb}=V_{ox}(R,N_a,t_{ox},W_d)+\phi_s(R,N_a,W_d) \qquad (5)$$

where $V_{fb}$ is the flat-band voltage. Using (5), depleted region width under the gate is expressed as follows

$$W_d=F(R,N_a,t_{ox},V_g,V_{fb}) \qquad (6)$$

Threshold voltage of PD-SGT is given by

$$V_{th}=V_{fb}+2.03\phi_B+\frac{qN_aW_d(2R-W_d)}{2\varepsilon_{ox}}\ln\left(1+\frac{t_{ox}}{R}\right) \qquad (7)$$

where $\phi_B$ is fermi potential in the body region. Using (4) and (5), S-factor of PD-SGT is obtained as follows

$$S=S(R,t_{ox},W_d,T)=\frac{kT}{q}(\ln 10)\frac{dV_g}{d\phi_{s\min}}$$

$$=\frac{kT}{q}(\ln 10)\cdot\left[1-\frac{\varepsilon_s}{\varepsilon_{ox}}\frac{\ln(1+\frac{t_{ox}}{R})}{\ln(1-\frac{W_d}{R})}\right] \qquad (8)$$

where $\phi_{smin}$ is the minimum value of channel surface potential, k is the boltzmann constant and T is the temperature.

**Results.** Defining the threshold voltage as the gate voltage required for the surface potential $\phi_{inv}$ to be $2.03\phi_B$, the result of this model agree well with those of 3D device simulator [3]. Fig.2 shows the derivation flow for threshold voltage and S-factor of PD-SGT. Fig.3(a) and (b) show the $N_a$ dependence for threshold voltage and S-factor of PD-SGT (R=0.4um,L=0.6um,$t_{ox}$=160Å). The results of this model ($V_{th}$, S) agree with those of 3D device simulator within 2.5% error and 0.7% error in maximum, respectively.

**Conclusions.** This paper proposes a new accurate model for threshold voltage and S-factor of PD-SGT. The results of this new model agree well with those of 3D device simulator. This new accurate model is very usefull for ULSI's design using PD-SGT.

## REFERENCES

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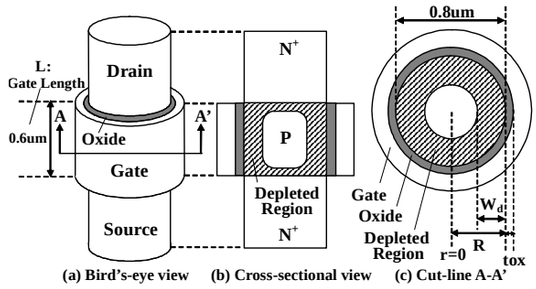


Fig.1 The structure of PD-SGT

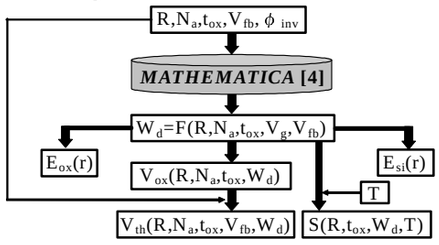


Fig.2 Derivation flow for $V_{th}$ and S-factor of PD-SGT

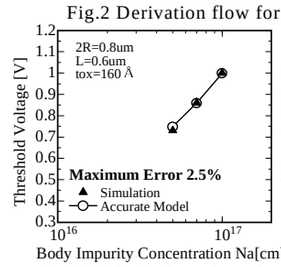


Fig.3(a) The $N_a$ dependence for threshold voltage of PD-SGT

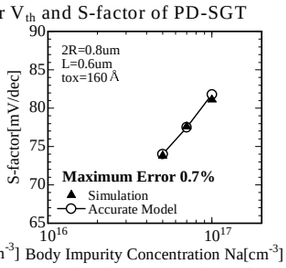


Fig.3(b) The $N_a$ dependence for S-factor of PD-SGT