THE NANOSCALE DOUBLE-GATE MOSFET FOR ANALOG APPLICATIONS

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There is a trend, for the analog and radio frequency transistors, to reuse the mainstream, digital CMOS technology to remain low cost and meet the demands for high-performance and reliability. It seems, therefore, very probable that analog circuits at the end of the roadmap will be typically built with the technology that results from the digital needs. Assuming that future analog circuits will be based on high-performance digital transistors, the question that naturally arises is, what are the expected parameters of these transistors concerning analog applications? The Double-Gate (DG) MOSFET provides the electrostatic integrity needed to scale devices down to their limits, reducing the short-channel effects, and will be used as a vehicle for our study. Previous studies about digital performance of the DG-MOSFET near the ultimate scaling limits have been done [1], but the analog performance has not been yet properly considered. To solve this question we report here the expected values of some relevant parameters for the analog circuit design, like the transconductance, transconductance efficiency, output conductance, and Early voltage. Results are reported in the ballistic and diffusive regimes by using the Non-Equilibrium Green's Function Method and the scattering theory of the nanoscale MOSFET. For this investigation we have selected a set of DG n-channel MOSFETs with metallurgical gate lengths (L) ranging between 10-30 nm. The International Technology Roadmap (ITRS-2001) requirements for the years 2006-2016 high-performance logic technology have been used as a guide for the design of these devices (Table I). One of the most remarkable results in this work is the very high transconductance (~20 mS/μm) reported for the 10 nm channel length DG-MOSFET (Figure 1), if the mobility is about 200-400 cm^2/V-s. We also observed that the maximum frequency of operation of the device is limited by thermal injection velocity to 2-4 THz. An important figure of merit in analog applications is the transconductance efficiency (Figure 2). For the 20-30 nm channel length DG-MOSFETs, with an ideal subthreshold slope, the transconductance efficiency approaches the bipolar limit in the weak inversion region (≅40 V^{-1}). If the channel length is reduced to 10 nm, short-channel effects degrade the transconductance efficiency to ≅30 V^{-1}. On the other hand, transconductance efficiency is not too much affected by temperature up to 373 K. Early voltage is severely affected by length scaling as channel length-modulation and drain-induced barrier lowering effects become more important (Figure 3), but acceptable values are obtained for channel lengths above 15 nm.

[1] Z. Ren et al., *IEDM Tech. Dig.*, Dec. 2001, pp. 5.4.1-5.4.4.

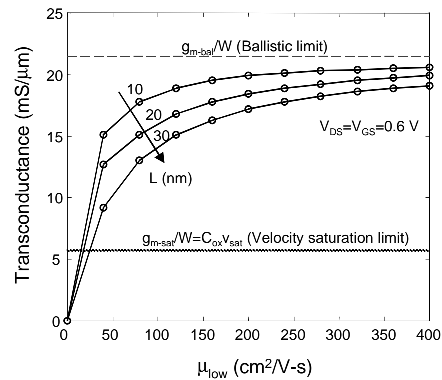

Fig. 1. Saturation transconductance versus low field mobility (solid line). In dotted line the drift-difussion limited transconductance is shown (no velocity overshoot is present). The ballistic limit for the transconductance is set by the thermal injection velocity from the source.

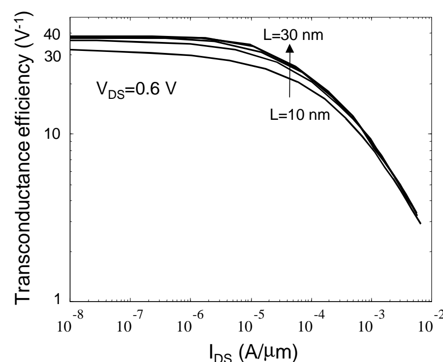

Fig. 2. Transconductance efficiency versus current for the ballistic regime.

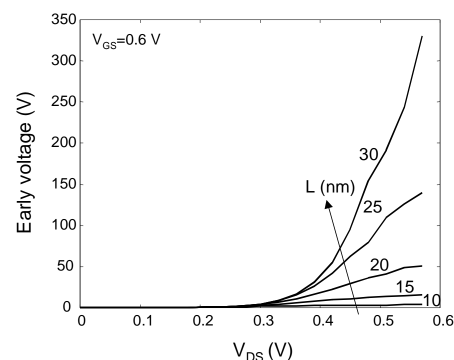

Fig. 3. Early voltage for different channel lengths considering the ballistic regime.

L (nm)	I_{off} (μA/μm)	I_{on} (μA/μm)	S (mV/decade)	V_{on} (mV)
10	4.4 (*10*)	5600 (*1500*)	75.6	180
15	0.17 (*7*)	4800 (*1500*)	64.8	200
20	0.06 (*3*)	4700 (*1200*)	61.7	214
25	0.04 (*1*)	4650 (*900*)	≅60	215
30	0.03 (*0.7*)	4600 (*900*)	≅60	215

Table I. Relevant digital parameters for a set of DG-MOSFETs with metallurgical gate lengths between 10-30 nm. The ITRS-2001 specifications for I_{off} and I_{on} are shown as a reference (values in parenthesis). (I_{off}=off-state current, I_{on}=on-state current, S=subthreshold slope, V_{on}=extrapolated threshold voltage).