The Benefit of SOI Technologies for Low-Voltage RFID applications

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RF identification (RFID) systems are currently under tremendous growth due to their wide application field (e.g. access control, luggage tracking …). To meet the market requirements, the technology that can be used for achieving such systems must enable small and low-voltage/low-power integrated circuits [1]. Thanks to their structure, the SOI technologies present several intrinsic properties for analog and RF applications. For instance, as it is well established now, these interesting devices allow the reduction of the power consumption at a given operating frequency. Moreover, the high insulating properties of SOI substrates, in particular with the use of high resistivity material, leads to high performance mixed-signal circuits. In order to investigate the suitability of CMOS/SOI for these applications, analog front-end circuits and a complete mixed-mode ASIC, operating at 13.56 MHz, for a long distance multi-tag RFID system have been designed and fabricated. All circuits have been mounted on a tag for connection to an external inductive loop antenna and have been tested in remote-power mode.

The circuits were fabricated using 0.25 µm LDD N-and P-channel Partially Depleted MOS/SOI transistors fabricated at the CEA/Léti (Grenoble) on 200 mm Unibond substrates. Front oxide thickness was T_{ox1}=4.5 nm, back oxide thickness T_{ox2}=400 nm and silicon film thickness T_{Si}=100 nm [2]. This technology features three different types of layout: floating body, body-tie and body-contact devices, along with poly-diffusion capacitors and diffusion resistors. The DC threshold voltage is 0,6 V for N-type and -0,7 V for P-type transistors.
First, the DC performances of SOI MOSFETs have been demonstrated. Low-frequency noise, which can directly impact RF or analog integrated circuits, was thoroughly evaluated. A particular attention has been paid to the floating body effect that induces a kink-related excess noise, which superimposes a Lorentzian spectrum on the flicker noise [4]. Results will be shown in the extended paper. Then, to study the transistor threshold voltage matching properties, on-wafer measurements of several hundreds of body-tie and body-contact devices have been carried out. They allowed us to derive mismatch versus device area plots. The results agree with classical data from the bulk CMOS literature, which prove the technology maturity.
The design and testing of circuits dedicated to RF identification are reported. Device level simulations have been achieved with the LETISOI model [3]. The analog front-end circuits (Fig. 1) show good power and clock recovery performance, due to the low voltage features of the technology. The tag-to-reader range is significantly improved compared to a 0.6 µm bulk CMOS reference chip.

The complete RFID chip, called ASTRAL1, has been designed for half-duplex communication between a remote-powered tag and a reader (Fig. 2). The digital part is used for identification, (de)coding/(de)modulation. Three anti-collision algorithms are also implemented for multiple-tag handling. Measurements proved the chip functionality and the suitability of the technology for lower voltages. It is worth noticing that, to our knowledge, it is the first mixed-mode CMOS/SOI chip dedicated to RFID.

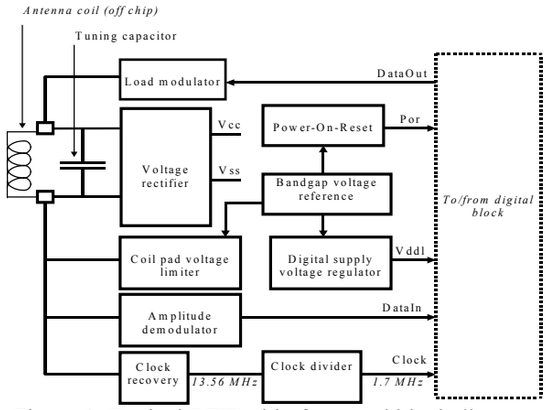

Figure 1: Typical RFID chip front-end block diagram

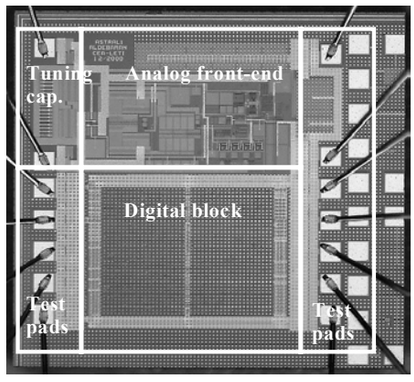

Figure 2: Chip microphotograph – ASTRAL1

Conclusion

An extensive study has been carried out on a 0.25 µm partially-depleted SOI CMOS technology. It goes from device level characterization to mixed-mode circuit applications. Low-voltage/low-power features of SOI technologies make them a promising solution for future RF or RFID developments.

Acknowledgment

This work is part of the Aldebaran project which was partially funded by the French Ministry of industry.

References

[1] D. Save "SOI for Smart Cards and RFID IC's", Silicon On Insulator Developments and Applications Workshop (Altis Semiconductor, SOITEC) September 6th-7th 2000
[2] J.L. Pelloie et al. "CMOS/SOI technologies for low-power and low-voltage circuits", Microelectronic Engineering vol.48, 1999, pp. 327-334
[3] O. Faynot et al. "Compact analytical modeling of SOI partially depleted MOSFETs with LETISOI", Solid-State Electronics vol.45, 2001, pp. 599-605
[4] S. Haendler et al. "Kink-related excess noise in deep submicron PD and FD Unibond N-MOSFETs", JJAP, Part 1, vol. 39, N° 4B, 2000, pp. 2261-2263.