Back-end Analysis of SOI Substrates Incorporating Metallic Layers using a Novel Non-destructive Picosecond Ultrasonic Technique

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ABSTRACT

The incorporation of buried metallic layers in silicon on insulator (SOI) substrates has proven and promises to yield significant enhancements to device performance. Tungsten silicide (WSi) used as a buried conduction layer under the active SOI (SSOI) has shown a reduction in collector series resistance in HBT bipolar transistors, increasing the speed (Fig.1).

A further application, which is attracting great interest, is the incorporation of a conductive, electrically isolated WSi ground plane layer into the SOI substrates (GPSOI), Fig. 2. The effect of such a conductive, grounded layer is to eliminate lateral voltage variations and hence the coupling of signals from one region to another. Using standard cross talk transmission test structures, it has been shown that substrates incorporating a WSi_2 GP layer can exhibit a 20dB improvement in cross talk suppression compared to the previous best results published for frequencies up to 30GHz.[1]

However, the incorporation of an opaque metallic layer has made traditional methods of SOI analysis such as ellipsometry, reflectometry and infrared (IR) inspection unsuitable. In this work, it is shown that picosecond ultrasonic technology (PULSE) can be used as a non-destructive post fabrication check, to determine the thickness and the integrity of all the layers that comprise the SSOI substrate, in particular the WSi_2 layer.

If the SOI substrates incorporating WSi_2 are exposed to very high temperatures T > 1150°C, the integrity of the WSi_2 layer can be compromised. Surface migration of silicon through the WSi_2, results in the formation of WSi_2 islands by an agglomeration process, to produce layer discontinuities, as can be seen in Fig. 3. Thus, the enhancements to device performance achieved by WSi_2 incorporation can be lost. Previously, the agglomeration of the WSi_2 layer could only be identified by a time consuming and destructive SEM/TEM analysis of the substrate. It has been suggested that PULSE measurement technology can be used to determine bond strength and bond integrity, and in this study we demonstrate that the technology can detect processing damage in the buried WSi_2 layer due to excess thermal budget.

In this study SSOI substrates were annealed at 1100°C, 1150°C and 1200°C, and the effect of the anneal on the buried WSi_2 layer was investigated using SEM and PULSE techniques.

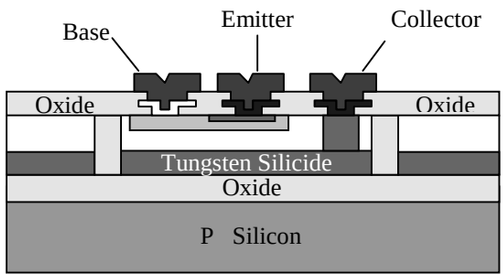

Fig. 1 HBT Bipolar Transistor fabricated on SOI incorporating a buried tungsten silicide conduction layer (SSOI).

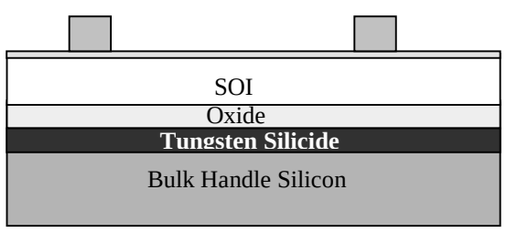

Fig. 2. SOI incorporating a tungsten silicide ground plane (GPSOI). The metallic layer electrically isolated from the SOI is grounded, shielding the bulk silicon from electric fields.

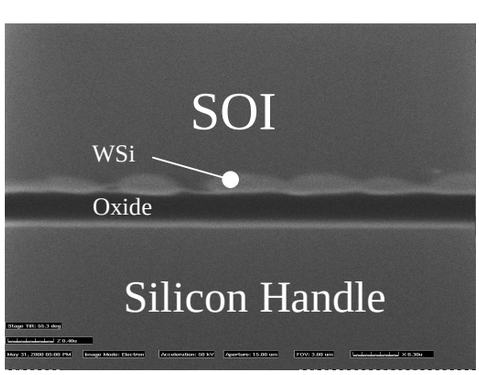

Fig. 3 Cross section of an SSOI where the WSi layer has broken up due to excess thermal budget.

References

1. J.S Hamel, S. Stefanou, M. Bain, B. S. Armstrong and H. S. Gamble. IEEE Microwave & Guided Wave Letters, V10, n 4, p 134-135 April 2000.