Comparison of SOI, Poly-Si TFT and bulk Si MOS performance using gm/ID methodology

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INTRODUCTION

Low temperature poly-Si TFTs are one of the SOI families. They recently achieve higher performance and integration onto glass substrate, aiming at system-on-glass (SOG). However, in the TFT analogue circuit fields, a systematic design methodology is still lacking. Here we extend the gm/ID methodology to TFT and use it to compare SOI, poly-Si TFT and bulk Si technologies.

Gm/Id methodology

Our design methodology [1] combines a behavioral analysis of the analog circuit at the symbolic level with the use of the transconductance-to-current ratio (gm/Id), which is a representation of the device behavior independent of device sizing. This method gives easier insight look of analog circuit and faster synthesis.

REVISION OF EKV MODEL FOR TFT

In the gm/Id methodology, EKV model is often used because of its simple formulation and suitability to analog design. However, the grain boundary trap effects inside the poly-Si TFT channel prevents direct application of EKV model to TFT. To deal with this trap effect, we developed a revision of EKV model.

(1) Threshold voltage

When the gate voltage is increased, the induced charge in the channel is first trapped by grain boundaries, so that the free charge density remains low. The drain current starts increasing when the boundary trap is filled. Thus, in TFT, the conventional threshold voltage, which is extracted from drain current versus gate voltage curve, doesn't coincide with the beginning of inversion charge increase. We rather use in the model, the threshold voltage (V_{tc}) extracted from gate capacitance [2].

(2) Slope factor modulation

In TFT, the slope factor (or body effect factor) n is affected not only by body effect but also by trap effect. In sub-threshold region, traps make the slope softer and the slope factor larger. On the other hand, we confirmed that in strong inversion region, the slope factor of poly-Si TFT is about 1.08 from the threshold voltage extraction with back gate bias. We introduce the following modulation to achieve continuity of n through all inversion regions.

$$n = n_{weak} + \left(\frac{n_{weak} - n_{strong}}{2} \right) \cdot \{1 + \tanh[\alpha \cdot (V_G - V_{tc})]\} \quad (1)$$

where n_{weak} and n_{strong} is n for each region, α is a voltage dependency coefficient.

(3) Mobility modulation

The field effect mobility is also affected by traps, and should thus be modulated as follows

$$\mu_{eff} = \mu_o + \left(\frac{\mu_0 - \mu_1}{2} \right) \cdot \{\tanh[\beta \cdot (V_G - V_{tc} - \Delta V_1)] - 1\} \quad (2)$$

where μ_0 and μ_1 are the mobilities in high and low fields, β is a voltage dependency coefficient, and ΔV_1 is a shift voltage.

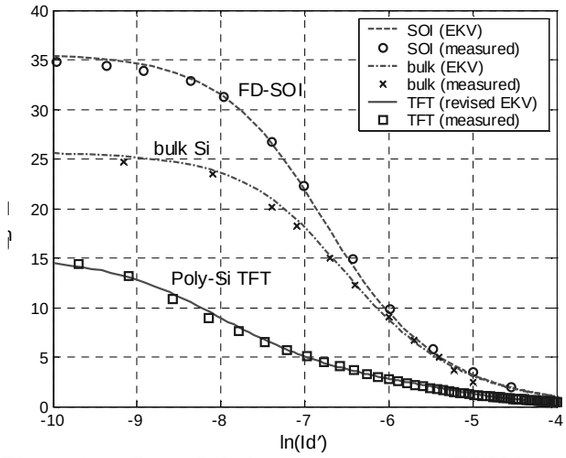

Figure 1 gm/Id vs. Id' of measurement and EKV for each technology

RESULTS

(1) Comparison of EKV & Measurement

Figure 1 shows gm/Id vs. Id' (=Id/(W/L)) curves for bulk silicon, SOI and poly-Si TFT MOSFETs. The symbols are measurements and the lines are from standard EKV (for SOI and bulk) and our revised EKV (for TFT). Each measured data curve shows good agreement with the models.

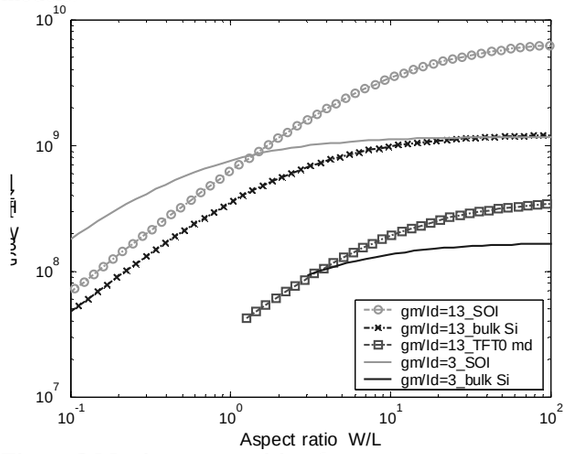

Figure 2 Maximum transition frequency vs. aspect ratio under fixed gm/Id & L with C_L=0.01[pF]

(2) Technology Comparison for amplifier performance

Figure 2 shows an example of common-source amplifier design by gm/Id methodology in consideration of junction capacitance. Maximum transition frequency (GBW) vs. aspect ratio (W/L) is plotted for gm/Id = 13 and 3 V^{-1}. The bulk Si shows earlier saturation of GBW than the other two technologies because of larger junction capacitance. Thus, the GBW difference between bulk and TFT becomes smaller in large frequency and aspect ratio region although TFTs still presently feature much lower mobility.

CONCLUSION

Thanks to a revision of EKV model, we can study poly TFT analog circuit by gm/Id methodology. Secondly, if the trap effect becomes smaller in future TFTs, these might even show higher analog performance than bulk Si because of smaller junction capacitance as in SOI.

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[2] M. D. Jacunski, M. S. Shur, M. Hack, IEEE trans. Electron Devices, vol. 43 (1999), 1433-1440.