Extraction of High Frequency Noise Parameters of 0.25µm Partially Depleted Silicon-On-Insulator MOSFET : Impact of the High Resistivity Substrate

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INTRODUCTION

The aim of this work is to analyse the impact of the substrate resistivity on the RF performances of 0.25µm n-channel partially depleted Silicon-On-Insulator MOSFET. As noticed in (1) and (2), the use of high resistivity substrate (10 kΩ·cm) seems to decrease the minimum noise figure (NF_{min}) of more than 1dB compared to devices tested on standard resistivity substrate (10 Ω·cm).

In addition, we explain why high resistivity substrate reduces noise. Therefore, we compare several intrinsic and extrinsic parameters with physical noise sources $\overline{i_g^2}$ and $\overline{i_d^2}$. These parameters provide accurate explanations of this result.

METHODOLOGY

The characterized devices are partially depleted SOI MOSFET with a 4.5nm thick gate silicon dioxide manufactured on 200mm Unibond® wafers. The buried oxide thickness amounts to 380nm while the upper silicon film thickness is adjusted to 100nm. Note that the process includes a titanium salicide step to reduce the gate access resistance.

The methodology takes into account the S-parameter and high frequency noise measurements of several devices on standard and high resistivity substrates. In that way, two measurement set-ups were used. The main parasitic contribution of pads and access lines on S-parameters is removed by a general de-embedding procedure. Next, extrinsic and intrinsic parameters were extracted from these on-wafer measurements using an extraction method as explained in (4).

A de-embedding procedure using the Hillbrand equations (3) was used to evaluate the noise parameters of the device without pads contribution. Then, we are able to extract the four noise parameters of the transistor itself and, with the help of admittance correlation matrix, the two noise current sources $\overline{i_g^2}$, $\overline{i_d^2}$ and the correlation between these noise sources.

RESULTS

After the extraction of the intrinsic parameters, results show a lower intrinsic minimum output conductance g_{dsmin} for the devices processed on high resistivity substrate than the standard resistivity ones (see fig. 1). We can notice a difference of 1dB between MOSFET SOI with high resistivity substrate and standard resistivity substrate at 8GHz (see fig. 2). The best results for the devices with high resistivity substrate can be explained by an impact of g_{dsmin} on the minimum noise figure. However, we have observed that the output capacitance C_{ds} have also an influence on the high frequency noise level (see table 1). This capacitance is more important for devices with high resistivity substrate. It means that there's a correlation between drain capacitance, substrate resistivity and noise.

These results show clearly the impact of the substrate resistivity on the high frequency noise performances (see table 1).

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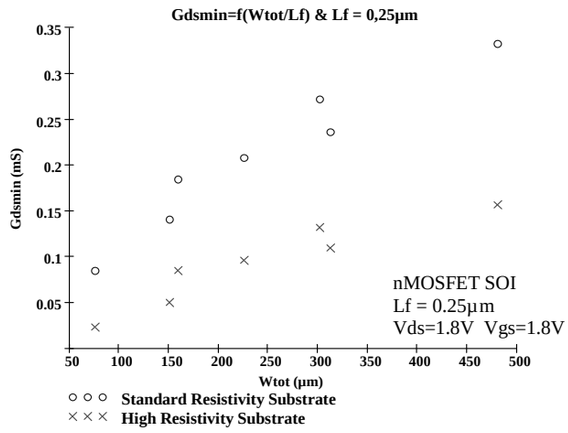

Fig. 1: Minimum output conductance versus gate width

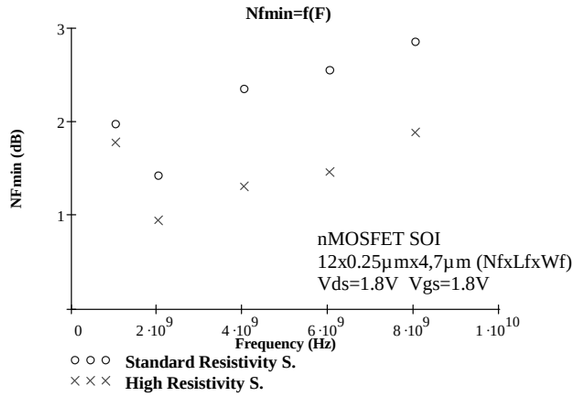

Fig. 2: Measured NFmin for nMOSFET SOI with high resistivity substrate and standard resistivity substrate

Substrate	**V_{ds}** (V)	**Jds** (mA/mm)	**L x W** (µm x µm)	***f*** (GHz)	**NFmin** (dB)	**Cds** (fF)
High R. p.d. (1)	1.8	35	0.18x200	2.5	1.0	-
High R. f.d. (2)	1.5	33	0.25x300	2	0.4	-
High R. (our work)	1.8	85	0.25x56.4	2	0.9	9
Std R. (our work)	1.8	85	0.25x56.4	2	1.4	11.5

f.d. = fully depleted; p.d. = partially depleted

Table 1