FEASIBILITY OF SURFACE PHOTO-VOLTAGE BASED CHARACTERIZATION OF ULTRA-THIN SOI WAFERS

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While SOI technology is undergoing unprecedented growth, electrical characterization of SOI wafers is facing serious challenges. This is due to the presence of buried oxide in SOI wafers, which renders standard methods of semiconductor substrate characterization mostly inadequate. The problem is further aggravated by the continued decrease of the thickness of the Si active layer, which will be scaled well below 100 nm in the next generation of fully depleted CMOS SOI devices.

Considering the cost of SOI wafers non-contact methods of electrical characterization are of particular interest since they would allow extraction of selected electrical characteristics of ultra-thin Si active layers in SOI wafers in a non-destructive fashion. One approach is to use AC Surface Photovoltage (AC-SPV) based methods [e.g. 1] for this purpose. In our earlier work [2] we have demonstrated that AC-SPV characterization techniques are suitable for SOI wafers on the condition that the active-layer thickness is larger than the sum of front and back depletion layers, i.e. the active layer is not fully depleted. The goal of this work is to evaluate feasibility of AC-SPV monitoring of fully depleted SOI wafers.

The total capacitance of a SOI wafer consists of those of the active layer, BOX and the depletion region in the substrate. In the case of a fully depleted active layer the only capacitance actually responding to the change in the charge in the BOX and active layer is that of the substrate depletion layer. While conventional capacitance measurements would yield the total capacitance of the wafer, the capacitance measured using AC-SPV is precisely that of the substrate depletion region. As a result the total charge present above the substrate, i.e. charge associated with BOX and Si active layer, may be determined. Providing the substrate doping is known the SOI structure can be now characterized.

To perform a meaningful characterization of SOI wafers a model is needed that will describe the influence of BOX and active layer parameters on the charge measured by AC-SPV methods. To this end an analytical model of charge interactions in a SOI substrate has been developed. The model is based on the assumption that all near-interface semiconductor regions are in depletion and that the active layer is fully depleted. The model describes the electrical state of the wafer depending on the wafer parameters, in particular the doping concentration of the active layer as well as the charges present at the surface and both Si/BOX interfaces.

In the full account of this work a complete model is introduced and discussed and the influence of BOX and active layer parameters on the charge measured by AC-SPV methods is considered in detail.

[1] E. Kamieniecki, G. Foggiato, “Analysis and control of electrically active contaminants by surface charge analysis”, in *Handbook of semiconductor wafer cleaning technology - science, technology and applications*, W. Kern (ed.), Noyes Publications, p. 497, 1993.

[2] L. Lukasiak, P. Roman, A. Jakubowski, J. Ruzyllo, “Analysis of surface and interface charge interactions in silicon on insulator (SOI) substrates”, Solid-State Electron., vol. 45, p. 95, 2001.