Analysis of Soft Errors in Floating Channel type Surrounding Gate Transistor (FC-SGT) DRAM Cells

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Abstract. This paper clarifies alpha-particle-induced soft error mechanisms in FC-SGT DRAM cells. Floating body effect is a significant factor to cause soft errors in floating channel type devices. The surrounding gate structure, however, can suppress the floating body effect compared with planer SOI DRAM cell. Therefore, FC-SGT DRAM is a promising candidate for future high density DRAMs having high soft-error immunity.

Introduction. In order to realize future high density DRAMs, three dimensional (3-D) structured SGT DRAM cell have been proposed [1]. The FC-SGT DRAM cell structure is shown in Fig.1(a). Gate, source, drain and plate are arranged vertically on a silicon pillar against the SOI substrate. As a result, FC-SGT DRAM can realize cell area of $4F^2$ per bit. DRAM design is also required high soft error immunity. The SOI substrate is expected as one of the countermeasures against the soft error [2]. However, soft errors in FC-SGT DRAM cells have not been reported until yet. This paper clarifies soft error mechanisms in the FC-SGT DRAM cell. Moreover, it is shown that FC-SGT DRAM cell has higher soft error immunity compared with SOI DRAM cell.

Soft errors in FC-SGT DRAM cells. A 3-D device simulation [3] was carried out under the "0" conditions shown in Fig.1(b). Device parameters are listed in Table I. Time-dependent current characteristics at the storage node and BL after the alpha-particle strike are shown in Fig.2. In phase I, the generated electrons are collected into the storage node or the BL due to the funneling and diffusion mechanisms. In phase II, the parasitic bipolar effect occurs in the emitter (storage node)–base (body)–collector (BL) structure. Electrons are transferred from the storage node to the BL. In phase III, the storage node and the BL currents are decreasing gradually. Using Fig.3, the parasitic bipolar effect is studied in more detail. Until about 40ps after the strike, the body potential continues to rise because the generated holes in the silicon pillar are swept into the body region. After the storage node junction is forward-biased, the body potential is constant until about 100 ns, because the amount of the holes accumulated in the body region is almost constant. Therefore, the parasitic bipolar current is constant. After about 100ns, the storage node junction is less forward-biased. This is because the storage node potential is raised by the electron ejection due to the parasitic bipolar current and the accumulated holes begin to disappear due to the recombination process. Fig.4 shows time-dependent potential characteristic at the storage node for the FC-SGT DRAM cell and the planer SOI DRAM cell using the same design rule. These results show the parasitic bipolar effect is a significant factor to cause a soft error in both cells. FC-SGT DRAM cell, however, can suppress the loss of the signal charge due to the parasitic bipolar current compared with SOI DRAM cell. This is because the body potential is strongly controlled by the surrounding gate and floating body effect can be suppressed.

Conclusion. This paper clarifies alpha-particle-induced soft error mechanisms in FC-SGT DRAM cells. FC-SGT DRAM cell can suppress the floating body effect compared with planer SOI DRAM cell. Therefore, FC-SGT DRAM is a promising candidate for future high density DRAMs having high soft-error immunity.

REFERENCES

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Table I Device parameters

L	Channel length	0.18 µm
T_{OX}	Gate oxide thickness	6 nm
R	Silicon pillar's radius	0.09 µm
N_D	Impurity concentration of diffusion layers	10^{20} cm^{-3}
N_A	Impurity concentration of body region	10^{18} cm^{-3}
C_S	Storage capacitance	30 fF
R_S	Resistance for the floating bias condition	10^{20} Ω

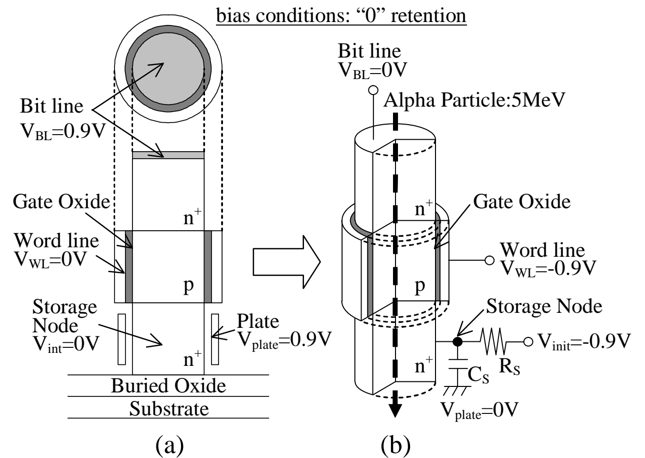

Fig.1 The structure of (a)FC-SGT DRAM cell and (b)the conditions used in a 3-D device simulation

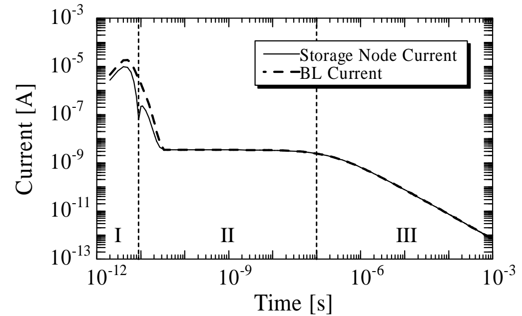

Fig.2 Time-dependent current characteristic at the storage node and BL after the alpha-particle strike

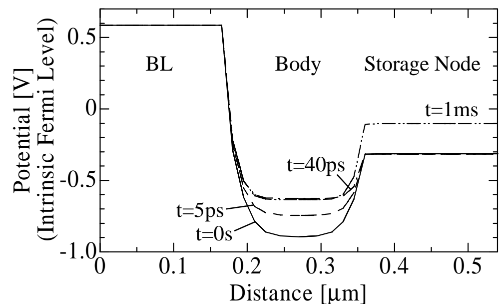

Fig.3 Cross-sectional potential profiles along the surface of the silicon pillar for FC-SGT DRAM cell

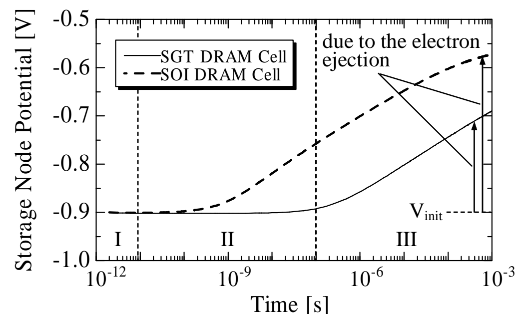

Fig.4 Time-dependent potential characteristics at the storage node for FC-SGT DRAM and SOI DRAM cells