Radiation Damage in Deep Submicron Partially Depleted SOI CMOS

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Introduction

The Commercial Off The Shelf (COTS) approach currently pursued by the space electronics community goes hand in hand with technology scaling. In other words, due to the reduction of the gate dielectric an implicit hardening has been achieved which brings commercial microelectronic components within the range of space applications, eliminating the need for costly technology hardening. At the same time, it has become clear that for the sub 100 nm era, Silicon-on-Insulator (SOI) is entering mainstream technology [1], indicating that it is no longer restricted to niche markets. Combining these two trends, the question emerges whether deep submicron SOI CMOS is suitable for operation in a radiation environment. Therefore, in this paper, the impact of 8 and 60 MeV proton and ^{60}Co γ-irradiation on the operation of Partially Depleted (PD) SOI MOSFETs, fabricated in a 0.13 µm technology, is investigated. It will be shown that while the integrity of the 2.5 nm NO gate oxide is largely maintained after the exposure, some peculiar irradiation-bias dependent back-gate damage effects occur in n-channel transistors, which reduce the generation lifetime in the silicon film.

Experiments and Analysis

Irradiations have been performed on PD SOI n-MOSFETs fabricated in a 0.13 µm SOI process, using a Polysilicon Encapsulated Local Oxidation of silicon (PELOX) isolation scheme, a 2.5 nm Nitrided gate Oxide (NO), 150 nm polysilicon gate and 80 nm nitride spacers. Devices with and without a halo implantation have been studied. Both mounted and non-mounted test structures with common gate/common source configuration and separate drain pads and no film contact have been investigated. The packaged devices were irradiated under bias (+1.5 V to the gate electrode and all other terminals grounded), while the diced chips had their contacts floating. 60 MeV proton irradiations were performed at a fluence Φ of 1x and $5\text{x}10^{11}$ p/cm^2, while Φ=$2.7\text{x}10^{12}$ and $2.7\text{x}10^{13}$ p/cm^2 for the unbiased 8 MeV exposures. For comparison, 13.5 and 100 krad(Si) γ-irradiations (no bias) were performed, to separate ionization effects from displacement damage.

The input and output characteristics of the devices have been studied prior to and within maximum two days after the irradiations. Besides the traditional parameters like the subthreshold swing, the threshold voltage V_T and the maximum transconductance g_{mmax}, the generation lifetime in the silicon film has been also studied, relying on the transient behavior of the switched off drain current [2,3]. Special attention was also paid to the impact on the so-called linear kink effect (LKE) and associated noise peak [4].

Results and Discussion

It will be demonstrated that in the first instance, the integrity of the NO oxide and interface is not changed after the different kinds of irradiation. This follows amongst others from the similar subthreshold slope and gate-induced drain leakage (GIDL) current and from the Capacitance-Voltage characteristics of large-area MOS capacitors fabricated in bulk wafers, belonging to the same batch. Occasionally, some trace of Radiation Induced Leakage Current (RILC) is found in the gate current at small gate bias, after 60 MeV protons, pointing to the creation of neutral electron traps in the NO dielectric.

Generally, a slight increase of the V_T and the g_{mmax} of the n-MOSFETs has been observed, which becomes more pronounced for shorter device lengths. These changes are irrespective of the type of irradiation and are in line with results obtained on 0.13 µm bulk CMOS transistors [5].

The most interesting feature is the impact of bias during 60 MeV proton irradiation on the subthreshold drain-body leakage. While unbiased n-MOSFETS show the creation of a subthreshold current hump, which is typical for conduction along the PELOX edges, a strong increase of the drain-body leakage current is found for the biased n-type devices. Associated with the enhanced device leakage is a faster switching-off drain current transient. The latter points to a reduction of the hole generation lifetime in the silicon film by either created isolation-edge or back-gate damage (interface states – surface generation velocity) or bulk damage in the diode depletion region. It will be shown that the enhanced carrier generation also affects the LKE effects (second g_m maximum and noise peak).

It should finally be remarked that the p-channel transistors exhibit far less device degradation than their n-MOS counterparts, which is expected from irradiation studies on 0.13 µm bulk CMOS [5]. No important impact of the presence of a halo was observed in the radiation response of the n-MOSFETs.

Conclusion

It has been shown that 0.13 µm PD SOI CMOS is radiation hard for space applications. A further hardening of the technology may result from replacing the PELOX by Shallow Trench Isolation. Some specific radiation-bias dependent back-gate-damage effects have been found, which have not been observed for bulk CMOS and require further studies for a full understanding.

References

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