Control of SEU in SOI SRAMs Through Carrier Lifetime Engineering*

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Single Event Upsets (SEU) have been of great concern in the stability of space SRAMs for a long time, and are increasingly so in commercial ones. They are caused by the charge generated and collected in the device sensitive regions by incident alpha particles and cosmic ray neutrons. This implies that the most fundamental method to control them is to reduce the SEU-sensitive volume, although a number of suitable circuit techniques have also been used. This is why, inherently small SEU sensitive volume SOI technologies have long been used for SEU-hardened SRAMs and other circuits: the SEU-sensitive volume in SOI MOSFETs is widely thought to be limited to the SOI film region under the gate (see however [1]). However, the floating body effects (FBE) and the implied parasitic bipolar transistor (BJT) meant that in order to materialize all the expected advantages originating from the reduced sensitive volume it is essential that the strength of the FBE be minimized. In practical terms this means to either tie the body to the source, or find ways to reduce the lateral parasitic BJT β. Body ties have been shown to provide limited efficiency in suppressing the transient FBE relevant to SEU and at the expense of complicated processing, whereas elaborate circuit techniques increase the area and degrade the performance. Moreover, in the case of body ties, the distance between the body-tie and particle impact location determines what part of the parasitic BJT will turn on, the associated series resistance, and ultimately leads to a wide and unpredictable spread in the values of β. Hence the need to reduce the gain β of the parasitic BJT without degrading the SRAM performance, best accomplished by controlling the carrier lifetime of the SOI film.

Two sets of devices (I and II) were fabricated on 0.35 μm PD SOI technology with t_{ox}=8 nm, t_{Si}=210 nm, t_{BOX}=400nm, and channel doping of about $3.3x10^{17}/cm^3$. Control devices I are used for comparison with devices II, which underwent a lifetime killing processing step to control their SEU vulnerability. These two sets of devices have different β values as shown in Fig. 1(a) and 1(b). Device I has β value ~8-10, twice than that of Device II, in accordance with the use of "carrier lifetime killing" used for devices II but not devices I. That this β control is indeed caused by "lifetime killing" was verified by the subsequent direct measurements of the generation [2] and recombination [3] lifetimes of both types of devices. In this measurement, the front interface of the NMOS is maintained in strong inversion by applying $V_{Gf}>V_T$ and the backgate (V_{Gb}) is pulsed from depletion to accumulation or from accumulation to depletion with a small positive applied to the drain. From the resulting drain current transients, one can form two generic Zerbst-type relationships for extracting the carrier generation (τ_g) and recombination lifetime (τ_r). From Fig.2 (a) and (b) it is found that for Devices I and II, τ_g values are ~8μs and 0.9 μs, respectively. Device II showed a lower τ_r (~10 ns) value compared to Device I (~20ns), consistent with the fact that a lower τ_r reduces the parasitic BJT effect.

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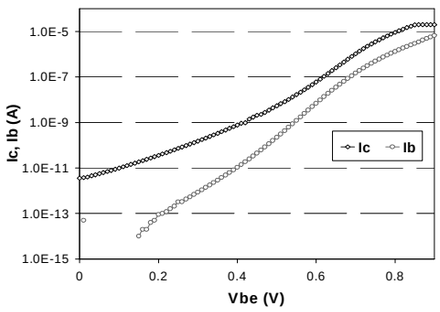

Fig.1 (a) Typical Ic and Ib curves for Device I

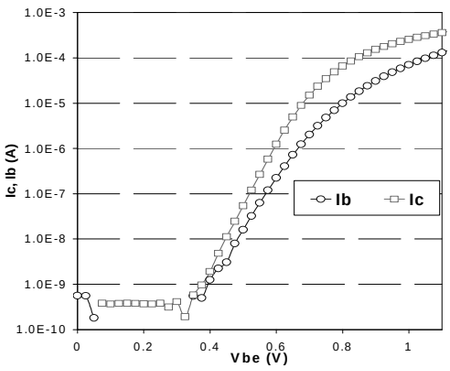

Fig.1 (b) Typical Ic and Ib curves for Device II

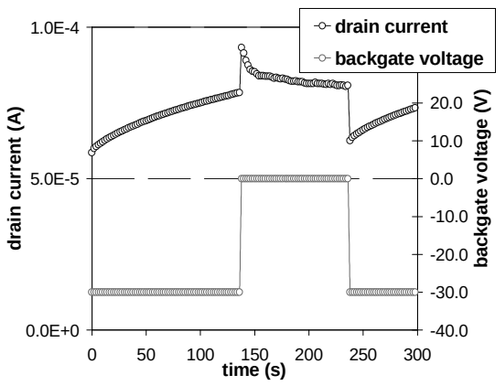

Fig.2 (a) Drain current and backgate voltage transient for Device I

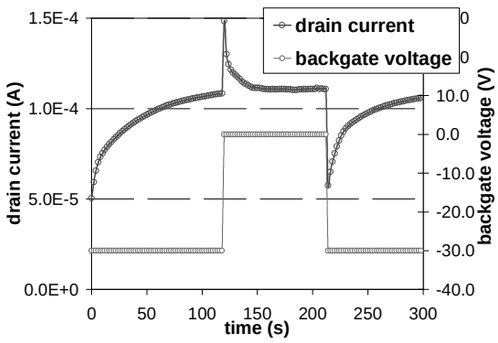

Fig.2 (b) Drain current and backgate voltage transient for Device II

References:
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[2] D.E. Ioannou et al., IEEE EDL-11, p.409, Sept. 1990
[3] D. Munteanu et al., IEEE TED-45, p.1678, Aug. 1998