# Very low Schottky barrier to $n$-type silicon with PtEr-stack silicide


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## 1. Introduction

Recently, the Schottky-barrier MOSFET has been proposed as an alternative to traditional MOSFET for sub-100nm devices because of its low source/drain contact resistance and swallow source/drain junction, which can effectively prevent the short-channel effect and suppress the floating-body effect. To obtain a higher current drive, lower Schottky barriers are required in this kind of device. Although Er has the lowest Schottky barrier to $n$-type silicon, it potentially exhibits severe oxidation problems that, in turn, induce strong contact resistance and kill the performance gain expected from the low intrinsic resistivity of $ErSi_2$. Thus processing Er silicide requires UHV deposition and annealing which adds strong constraints in the MOSFET application. To solve that problem, a Pt layer was deposited on top of Er layer to protect the later from oxidation. We investigated the as a viable solution for the erbium silicidation step. The results show that the PtEr-stack silicide is a good candidate for the $n$-channel Schottky-barrier SOI-MOSFET.

## 2. Results and discussion

In a real Schottky-barrier MOSFET, current flows through two Schottky diodes separated by a silicon series resistance. To reproduce this lateral configuration, two Schottky contacts were produced on $n$-type silicon by the successive deposition of a 50nm-thick Er layer and a protecting 40nm-thick Pt layer. Then this system was annealed at 600°C for 2min by RTA. When an external voltage V is applied to the drain terminal, the drain Schottky diode ( $D_d$ ) is reverse biased and the source Schottky diode ( $D_s$ ) is forward biased. The voltage drop across $D_s$ is negligible compared to that across $D_d$ . Hence, the barrier of the drain Schottky diode controls the maximum current drive. In the thermionic emission theory, the reverse saturation current, $I_o$ is given by:

$$I_o = AA^* T^2 e^{-\frac{q\phi_B}{kT}} \quad [1]$$

With the help of an Arrhenius plot, where $\log(I/T^2)$ is plotted vs. $1/T$, the drain Schottky barrier height $\phi_B$ can, in principle, be determined.

Figure 1 shows the I-V curves taken at different temperatures for a PtEr-stack silicide system on a $n$-type silicon substrate with a concentration of $1.4x10^{16}cm^{-3}$ in the active region. In the temperature range from 110K to 200K, the I-V curves show a non-linear behavior and the current increases with increasing temperature. This implies that the reverse-biased Schottky contact limits the current. However, the current does not saturate at large voltages due to the barrier lowering and the field emission mechanisms. Both mechanisms can significantly enhance the current level compared to prediction of pure thermionic emission model and can affect the accurate determination of very low barrier height. Fortunately, the additional current contribution does not affect the determination of the barrier height extrapolated in the limit of zero applied bias. The extracted barrier height near zero voltage is found to be smaller than 0.1eV, which is much lower than the lowest reported value of 0.27eV for the simple Er silicide system. The data in Fig. 1 show that the temperature dependence of the current reverses above 200K, while the I-V characteristics become linear. This indicates that the silicon series resistance limits the current. Figure 2 shows the cross-section of the system before and after an annealing. Layer boundaries are very regular before annealing, whereas the $ErSi_2$/Si boundary becomes undulated after annealing. SOI should solve that problem by limiting vertical diffusion to the buried oxide layer. It can be seen that the deposited Er (50nm) reacts with silicon to form an $ErSi_2$ layer with average 120nm-thick while Pt layer of 40nm-thick remains essentially unaffected. This consolidates the role of Pt as a protecting layer that prevents Er and $ErSi_2$ from oxidation, and does not penetrate into the silicide, which might have enhance the Schottky barrier height to n-type silicon, as it is the case for pure PtSi.

## 3. Conclusion

A PtEr-stack silicide was formed by the successive deposition of Er and Pt on a $n$-type silicon substrate with a concentration of $1.4x10^{16}cm^{-3}$ in the active region and annealed at 600°C by RTA. A Schottky barrier height near zero voltage smaller than 0.1eV has been observed. Hence the PtEr-stack silicide system is a potential candidate n-channel Schottky-barrier MOSFET as it exhibits a very low Schottky barrier to electrons while Pt protects the silicide from oxidation under non-UHV conditions. Since the Schottky-barrier MOSFET will be fabricated on SOI, the PtEr-stack silicide system will contribute to improve SOI technology in the future.

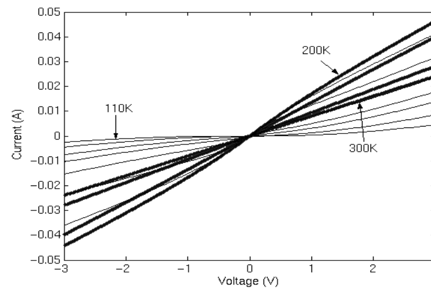


Fig. 1: Current-voltage characteristics from 300K to 200K (thick lines) and below 200K (thin lines).

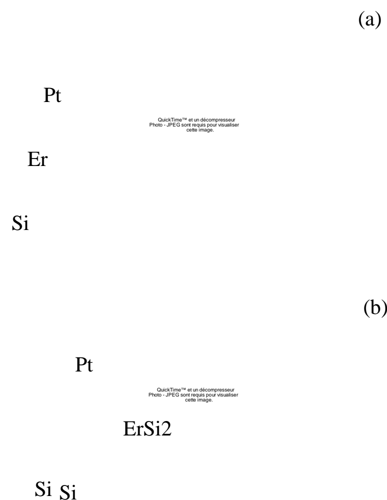


Fig. 2: TEM micrographs of the cross-section of the PtEr-stack silicide before (a) and after (b) annealing.