Figures-of-Merit of Intrinsic, Standard-Doped and Graded-Channel SOI and SOS MOSFETs for Analog Baseband and RF Applications

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INTRODUCTION

The choice between multiple threshold voltage (V_{th}) devices, more and more often available in CMOS processes, is not always obvious for analog designers and is often based on experience rather than on actual figures-of-merits. For design optimization, it is often required to trade-off highest cut-off frequencies vs lowest power consumption or highest gain performances. Such figures-of-merit of baseband analog and RF performances are discussed for standard doped (SD) and intrinsic (IN) transistors. Moreover, an asymmetrically doped nMOSFET (Graded channel MOSFET, GCMOS) is considered as another solution for increasing the analog performances. Two different technologies are used; the first one is a Silicon-on-Sapphire (SOS) 0.5 µm Fully Depleted (FD) technology, the second is a 0.5 µm Silicon-on-Insulator (SOI) technology.

RF PERFORMANCES

The transistors have been measured from DC up to 40 GHz using a vector network analyzer. After the de-embedding of the connecting pads using the method proposed in [1], the RF performances have been extracted. The transition frequency (f_t) which is defined as the frequency when current gain is equal to one, has been considered as RF factor of merit for comparison purposes. f_t is approximately given by $g_m/(2\pi C_{gg})$, where g_m is the gate transconductance and C_{gg} the total gate capacitance. Fig. 1 plots the normalized current (I_d/W) needed to achieve a f_t higher than 10 GHz for various transistors with a gate length of 0.5 µm and different DC gate biases. In the case of SOS devices, no significant difference appears in terms of current consumption when the IN and SD transistors are compared. However, lower gate voltage levels in the case of IN are of major interest in low-voltage applications in order to achieve input dynamic range enhancement in differential opamps. The use of GCMOS leads to significative decrease of the required current value due to its reduced effective channel length [2]. On the contrary to SOS devices, when comparing devices in SOI technology, it appears that the IN device requires significantly less current to reach a f_t higher than 10 GHz. Moreover the highest measured f_t was nearly 10% higher for the IN compared to the SD devices. This increase can be explained by the improvement of mobility for the intrinsic SOI devices as it is demonstrated in next section.

BASEBAND CHARACTERISTICS

In order to get physical insight and fair comparison of the effective analog performance between various devices from a circuit designer point of view, we introduce a graphical representation illustrating the relationship between the intrinsic gain A_{v0}, the gain-bandwidth product *GBW* (normalized to 1 pF load capacitance), the dimensions and the power consumption of the device.

Fig. 2 presents A_{v0} vs *GBW* for fixed dimensions, for standard and intrinsic 0.5 µm nMOS transistors both in SOI and SOS processes, and for 1 and 0.5 µm GCMOS in SOS. These curves were obtained from the measured g_m/I_d and Early voltage (V_{ea}) characteristics of 0.5 µm effective channel length (L_{eff}) transistors. GCMOS with L_{eff} of 0.25 µm (gate drawn length, L = 0.5 µm) was added for comparison with equal drawn gate length devices. Firstly, we show that intrinsic transistors yield very strong gain improvement in SOI, mainly due to a strong increase of their V_{ea}. Secondly, a maximum *GBW*, above which gain falls and current biasing becomes infinite, appears. This is linked to the maximum g_m of the different devices. It is higher in SOI, and for intrinsic device due to the mobility improvement with doping reduction. This also explains the better RF performances observed in Fig. 1.

In SOS, low doping does not bring any advantage since mobility is dominated by other scattering mechanisms. The lower GBW_{max} observed for GCMOS is related to a higher channel doping density for the measured devices and not to the asymmetric channel structure. It can be compensated by the reduction of L_{eff} by shifting the implantation mask of the GCMOS process. Finally, the gain improvement brought by GCMOS is evident. At identical *GBW* and L_{eff}, GCMOS presents up to a tenfold gain improvement compared to the corresponding SOS standard nMOS. For an equal gate drawn length (L), GCMOS still presents higher gain than the corresponding SD despite a two times smaller L_{eff}.

CONCLUSION

Based on actual figures-of-merit for analog/RF circuit performances, low-doped FD MOSFETs demonstrate a very intersting potential to lower power consumption and increase gain and frequency performance both on SOI, and to a lesser extent, SOS processes. Further significiant optimization can be obtained using the graded-channel device architecture for equal gate length.

REFERENCES

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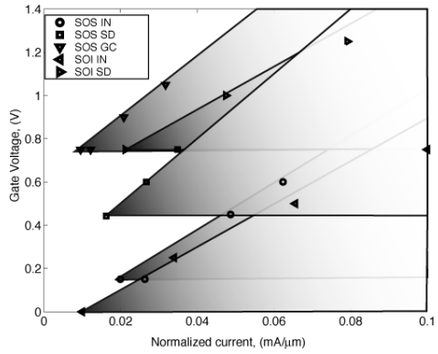

Fig. 1. Biasing conditions allowing to achieve a f_t>10 GHz.

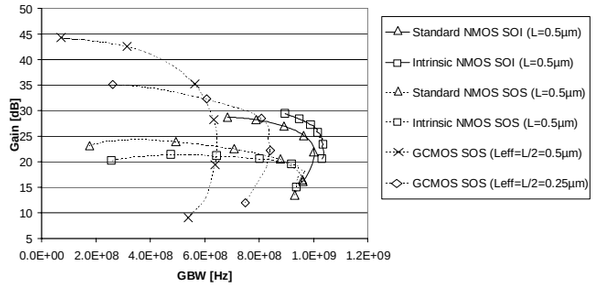

Fig. 2. A_{v0} vs *GBW* for fixed channel width W=50 µm, V_{drain}=1.2V and C_L=1 pF.