Comparative Study of the Dynamic Performance of Bulk and FDSOI MOSFET by means of a Monte Carlo Simulation

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Fully-Depleted (FD) Silicon-on-Insulator (SOI) MOSFETs are receiving a lot of interest in the last years due to their improved high frequency performance as compared to bulk devices. Nevertheless, it is almost impossible to perform experimental one-to-one comparisons between them due to the different geometrical and physical parameters of fabricated transistors [1Colinge]. In this work, we have employed an Ensemble Monte Carlo (EMC) simulator [2Yo mismo] to evaluate the differences on the static and dynamic characteristics of 0.25 µm bulk and FDSOI MOSFETs with equivalent topologies. This simulation technique allows to examine the effect of the buried oxide on the internal magnitudes of carrier transport (velocity, energy, carrier concentration, electric field profile, etc.). Furthermore, the parameters of the small-signal equivalent circuit (SSEC) can also be readily evaluated in terms of those magnitudes.

Two different values for the active layer thickness (t_{si}) have been considered in order to evaluate the influence of this parameter on the static behavior and the SSEC parameters The simulated bulk device topology remains equal with the exception of the absence of the buried oxide.

The slope of the transfer characteristic (Fig 1.a) is larger in the FDSOI than in the bulk yielding larger values of the transconductance, g_m. Furthermore, the narrower active region in the FDSOI MOSFETs as compared to the maximum depletion width in the bulk device induces a reduction in the threshold voltage (V_T) which is stronger for the lowest value of t_{si}. The reason for this behavior can be found in the internal magnitudes of the devices. In the FDSOI MOSFETs, an additional band bending (which is more pronounced for the thinner t_{si}) of the potential from the gate to the substrate has been observed. As a consequence, a thicker inversion layer is obtained for the FDSOI devices (Fig. 2.a), which increases with the reduction of t_{si}. Despite the higher transconductance found in the FDSOI devices, a degradation of this figure of merit appears when t_{si} reaches 30 nm. In this case, the reduced value of the thickness of the active layer yields to a higher value of the resistance associated to the source and drain regions, thus affecting the transport conditions in the channel. This is also clearly shown in the linear regions of the I_D-V_{DS} characteristics (Fig. 1.b), where a lower slope is observed for the FDSOI MOSFET with t_{si} = 30 nm. Furthermore, for FDSOI devices, significantly reduced values of electric field are found both in the *X* (along the channel) and *Y* (perpendicular to the channel) dimensions as compared to the bulk MOSFET (specially in the case of the electric field at the drain side of the channel). As a consequence, lower values for the electron energy are obtained in the pinch-off region, which would indicate a reduced effect of hot carrier degradation. The reasons for this behavior can be associated to the shape of isopotential lines, which indicates that in the case of FDSOI MOSFETs the buried oxide "absorbs" most of the potential drop from the gate to the substrate leading to gradual electric fields in the *X* and *Y* directions.

The SSEC capacitances for the three devices are shown in Fig. 2.b. First of all, is must be remarked the strong reduction of the C_{DS} capacitance of the FDSOI MOSFET transistors compared to those obtained for the bulk. This indicates a significantly reduced influence of coupling to the substrate, which is of great interest for high frequency applications. Regarding the C_{GS} capacitance, the higher values obtained for FDSOI devices (specially for t_{si}=30 nm) for V_{GS}- V_T greater than 0.5 V indicate a larger variation of the charge closer to the source due to the thicker inversion layer. As a consequence, lower values of the cut-off frequency are found for the FDSOI MOSFETs for the largest values of V_{GS} - V_T (Fig. 3).

In general, as expected, FDSOI MOSFETs offer an improved performance as compared to the bulk device in terms of g_m, lower electric fields and carrier energy together with an extremely reduced coupling to the substrate. Nevertheless, it must be remarked that a trade-off exists between the advantages obtained for FDSOI MOSFETs and the thickness of the active layer, specially in terms of the values of important figures of merit such as g_m and f_T.

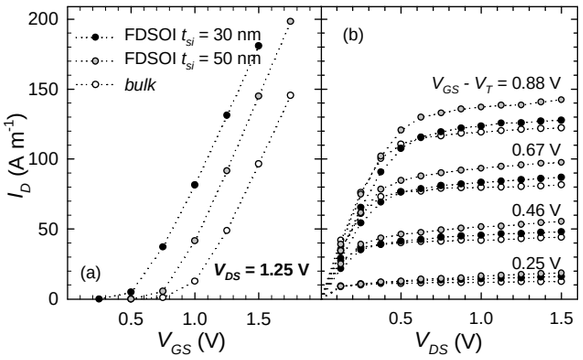

Fig.1. Transfer characteristic (a) and output characteristic (b) for a bulk MOSFET, FDSOI MOSFET with t_{si} = 50 nm y FDSOI MOSFET with t_{si} = 30 nm. Output characteristics correspond to the same V_{GS} -V_T conditions.

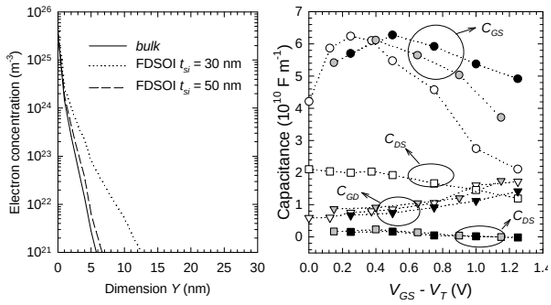

Fig. 2. Carrier profile of the inversion layer for V_{DS}=0 V (a). SSEC capacitances of the devices for V_{DS} = 1.25 V (b)

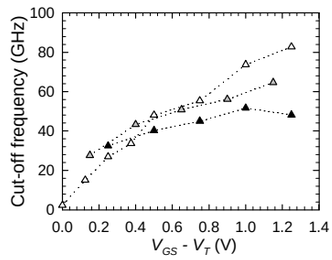

Fig.3. Cutt-off frecuency for the devices

[1] Colinge J. P. *Silicon-on-Insulator Technology: Materials to VLSI* 2nd edition (Norwell, MA: Kluwer, 1997)

[2] Rengel R et al., "Numerical and experimental study of a 0.25 µm fully-depleted silicon-on-insulator MOSFET: static and dynamic radio-frequency behaviour", *Semicond.. Sci Tech.* **17** p. 1149 (2002)