Threshold Voltage Quantum Simulations for Ultra-Thin Silicon-On-Insulator Transistors

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Introduction

In 2007 high performance MOSFETs will have to exhibit 25nm gate length, and aggressive performances [1]. Fully Depleted Silicon-On-Insulator transistors (FD-SOI) seem to be good candidates to fulfill the ITRS requirements because they show a good scalability compared to bulk devices. Since silicon film thickness (Tsi) will have to be lower than 10nm in these devices, quantum effects will affect transport properties and threshold voltage (Vt)[2].

The three operation states

As FD-SOI transistors are scaled down, thin films are used and the Poisson and Schrödinger equations have to be solved to determine the energy levels and the spatial distribution of the charges. In our study, this was carried out by using a finite element method [3]. Threshold voltage was extracted at constant charge. Vt=f(Tsi) for a nMOS transistor is reported in figure 1. Three behaviours can be observed : for thick films the transistor is Partially Depleted (PD). The threshold voltage is independent of the silicon thickness . For a high doping level case(bulk-like), a high surface electric field leads to important quantum effects. When the silicon thickness decreases, the transistor operates in a FD-SOI mode. Surface electric field and consequently electronic energy levels separation decrease. Therefore the Vt difference between classical and quantum calculation decreases. Finally, the use of a thinner film rises the spacing between the energy levels and then implies an increase in the threshold voltage : within the infinite level wells approximation the n^{th} energy level can be written as $E_n^{\infty}=(\pi^2\hbar^2/2m_e).(n/Tsi)^2$, where m_e is the electron mass and $\hbar$ Planck's constant.

Threshold voltage optimization

As a reminder the 65nm technological node requires a gate oxide thickness between 0,6 and 1,4nm and the supply voltage must be between 0,6 and 0,9V. As a consequence the threshold voltage will reach value as low as +0,2V/-0,2V for nMOS/pMOS.

N^+/P^+-like dual-gate

In order to minimize two-dimensional effects (short channel effects, DIBL), the silicon film thickness should not exceed 10nm for such a device. Simulations were performed for nMOS with Tbox=50nm, Tox=1nm. In the case of N+-like gate, high doping levels are required in the channel to reach a suitable threshold voltage of 0,2V (figure 2). Actually, for 5 to 10nm films, the doping level in the channel (Nch) will have to be close to 1e19at.cm^{-3}. That leads to mobility degradation and threshold voltage scattering due to doping fluctuation and film thickness dispersion. Let us consider a uniformly doped structure (with a Poisson's distribution), Tsi=10±3nm, Lg=25nm. σ is the atoms number standard deviation, ΔVt the threshold voltage standard deviation. We can reach a Vt dispersion almost as important as threshold voltage values for high doping levels (Table 1). As a consequence it will be difficult to use N^+/P^+-like dual-gate for gate length as short as 25nm.

From midgap gate to φ_M engineering

If we assume a midgap gate, threshold voltage as low as 0,2V cannot be reached, even if low channel doping levels are used (figure 2). Consequently 25nm gate length FD-SOI nMOS/pMOS require gate materials with φ_M values of -0,2eV/+0,2eV around the midgap to satisfy the ITRS.

Conclusion

For ultra-thin SOI, supply voltage decrease will lead to the use of φ_M engineered gate rather than N^+/P^+-like gate.

This work has been carried out, in the frame of CEA-LETI / CPMA collaboration, with PLATO Organization teams and tools

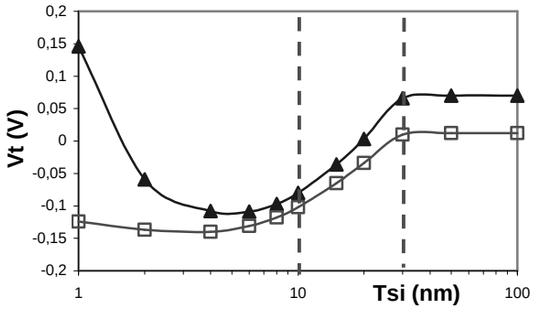

Figure 1 : Classical (square) and quantum mechanical (triangle) simulations. Nch=1e18at.cm^{-3}

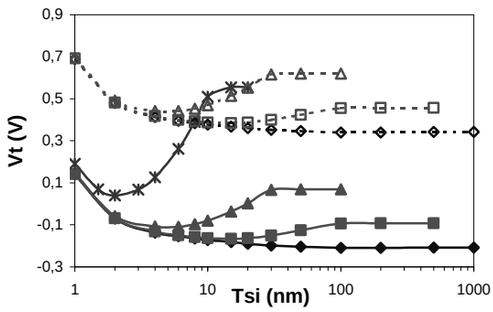

Figure 2 : $V_T=f(T_{si})$ for different channel doping level. Diamond : 1^{e}15 at.cm^{-3}, square : 1^{e}17 at.cm^{-3}, triangle : 1^{e}18 at.cm^{-3}, cross : 1^{e}19 at.cm^{-3}. Filled : n+ gate ; open : mid-gap gate.

Nch (at.cm^{-3})	1e19	1e18	1e17	1e16
n (at.)	2500	250	25	2.5
σ=√n	50	16	5	1.6
Nch[n ± 2σ] (at.cm^{-3})	[9.6e18; 1.04e19]	[8.7e17; 1.1e18]	[6e16; 1.4e17]	[0;5e16]
ΔVt (mV) ± 4σ	140	60	25	20

Table 1 : Threshold voltage dispersion for different channel doping level

[1] ITRS Roadmap 2001.
[2] Y. Omura, S. Horiguchi, M. Tabe and K. Kishi, « Quantum mechanical effects on the threshold voltage of ultrathin-SOI nMOSFET's » *Electron Device Letters*, Vol. 14, n°12, 1993 pp569-571.
[3] A. Poncet, C. Faugeras, and M. Mouis, "Simulation of 2D quantum effects in ultra short channel MOSFETs by a finite element method", *Eur. Phys. J. AP.* , Vol. 15, 2001, pp. 117-121.