60-nm gate length SOI CMOS technology optimized for "System-on-a-SOI-chip" solution

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Introduction

In this paper, we describe 60-nm gate length SOI CMOS technology for "system-on-a-SOI-chip" solution. This concept features that: 1) high-speed logic circuits are designed with the PDSOI in order to improve functional speed, 2) the remaining circuits which require stable body-potential are designed with the Body-slightly-tied SOI (BSTSOITM), in which body potential is fixed [1]. With newly developed self-aligned dual trench isolation (SDTI), both PDSOI and BSTSOI can be fabricated on the same die. We compare PDSOI and BSTSOI with bulk CMOS in terms of transistor characteristics and circuit performance. In addition, we demonstrate the stacked metal-insulator-metal (MIM) capacitor DRAM cell fabricated on BSTSOI [2].

Device structures

Fig.2 shows a schematic diagram of BSTSOI and PDSOI device structures having SDTI. PDSOI is surrounded by full trench isolation which reaches buried oxide (BOX) layer. On the other hand, BSTSOI is surrounded by partial trench isolation, in which SOI layer remains between BOX layer and trench isolation. Therefore body potential of BSTSOI is fixed with body contact via resistance path below the trench isolation. Fig.3 schematically shows process sequence of self-aligned dual trench isolation (SDTI). Here initial SOI thickness was 150 nm. First, partial trench (etching depth of 100 nm) was formed followed by thermal liner oxidation. Next, sidewall spacer was formed and well implantation into BSTSOI region was performed. This well implantation lowers body resistance, and enables isolation space (n+ to n+ or p+ to p+) shrinking in BSTSOI region. Then full trench, self-aligned with partial trench isolation using sidewall spacer, was formed. Transistor fabrication process after SDTI was based on 90-nm node bulk CMOS technology [3]. The equivalent oxide thickness of gate dielectric was 1.6 nm and gate length was 60 nm. The poly-SiGe gate and pre-doping technology were used for performance improvement. Final SOI film thickness under gate electrode was 130 nm.

Transistor and circuit performance

Fig. 4 shows DC output characteristics of PDSOI, BSTSOI, and bulk CMOS, all of them having the same channel and extension/halo implantation conditions. PDSOI shows kink in output characteristics due to floating body, while BSTSOI shows almost the same curves with those of bulk. We estimated self-heating effect (SHE) of the above these devices using AC drain conductance method [4]. Estimated drain current degradation by SHE were 2.7% for nMOS and 1.3% for pMOS in PDSOI (gate length of 60 nm, gate width of 1.0 µm at supply voltage of 1.2V). Those value were 2.3% for nMOS and 1.1% for pMOS in BSTSOI. Fig. 5 shows propagation delays of inverter gate and its standby leakage current as a function of supply voltage. Speed improvement of PDSOI over bulk CMOS is 23 %. However off leakage current of PDSOI is 4.5 times higher than that of bulk device because of larger DIBL due to floating body. On the other hand, BSTSOI has almost the same off leakage current with bulk device and its speed improvement over bulk is 7.5 %.

Embedded DRAM on SOI

Fig. 6 shows a schematic cross-section of DRAM cell on BSTSOI. This DRAM cell, which consists of silicided transistor and MIM capacitor, achieves extreme high-speed random access cycle of 570 MHz [2]. The body potential of DRAM cell is pinned with body contact so that we can use the same cell layout with that of bulk. Furthermore, there is no dead zone between BSTSOI and PDSOI boundary so that part of peripheral circuits can be selectively designed with high-speed PDSOI.

References

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[3] A. Ono, et al., VLSI Tech., pp. 79-80, 2001.
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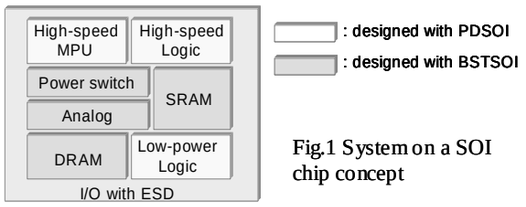

Fig.1 System on a SOI chip concept

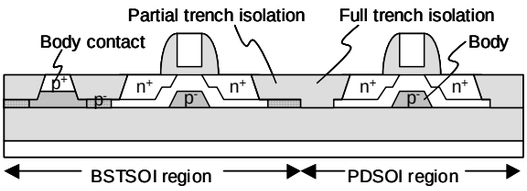

Fig.2 PDSOI and BSTSOI structures

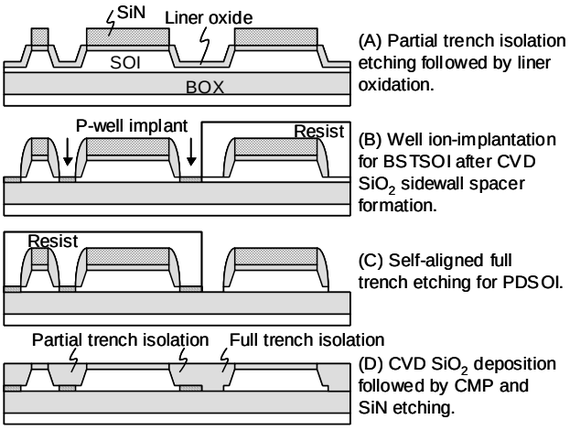

Fig.3 Process sequence of self-aligned dual trench isolation

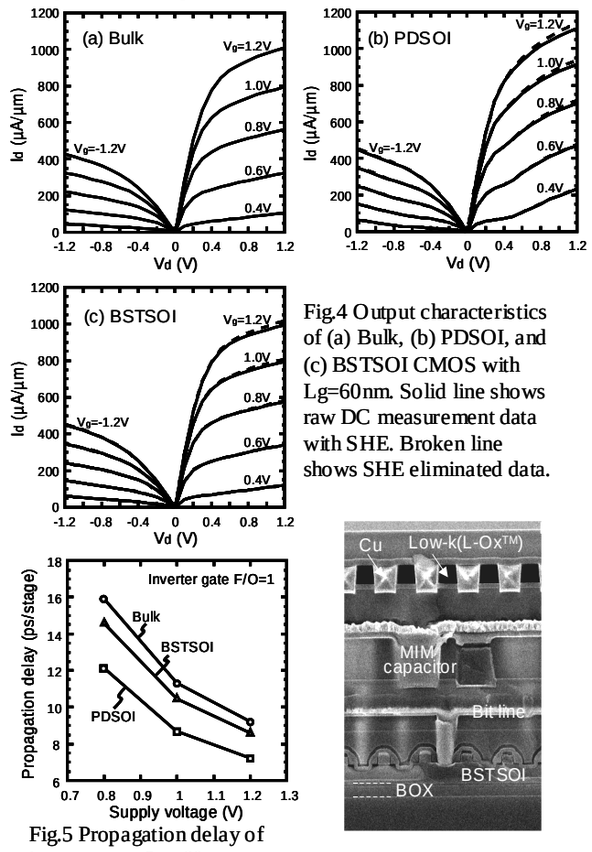

Fig.4 Output characteristics of (a) Bulk, (b) PDSOI, and (c) BSTSOI CMOS with Lg=60nm. Solid line shows raw DC measurement data with SHE. Broken line shows SHE eliminated data.

Fig.5 Propagation delay of inverter gate. Lg=60nm, Wn=0.9µm, Wp=1.44µm.

Fig.6 SEM view of embedded DRAM on BSTSOI.