Strained-Si/SiGe-on-Insulator CMOS Technology

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MOSFET with a high mobility channel is an attractive device structure, which leads to reduction in supply voltage with maintaining the high circuit performance. From this viewpoint, a strained-Si channel is promising for CMOS application [1], because of the high electron and hole mobility. However, strained Si CMOS on bulk substrates have the same obstacles as conventional Si CMOS, such as junction capacitance, junction leakage current and short channel effects. Thus, we have proposed strained-Si/ SiGe-on- Insulator (strained-SOI) MOSFETs to overcome these problems [2, 3]. This paper reviews our recent progress on the fabrication and device characteristics of strained- SOI CMOS.

Fig.1 shows the typical device structure of strained-SOI MOSFETs [2]. Particularly, by adopting fully-depleted (FD) structure having a thin SOI layer, strained-SOI MOSFETs become more attractive for sub-100 nm node CMOS, in terms of higher mobility, immunity to short channel effects and statistical variation of V_{th}. Other advantages than the simple combination of SOI structures and high mobility are (1) suppression of floating body effects due to hole current flow through SiGe pn-junction (2) lower self heating effect due to thinner SiGe layers (3) possible low dislocation density in relaxed SiGe due to slip at the interface between SiGe and buried oxide.

The most important process in fabricating strained-SOI MOSFETs is the preparation of thin and relaxed SiGe-On- Insulator (SGOI) substrates with minimal dislocation density. The main concept of our original approach to the SGOI fabrication [4], called the Ge condensation due to oxidation, is summarized in Fig. 2. This technique can apply to both bulk and SOI substrates with SiGe films.

When oxidizing SiGe layers on commercial SOI substrates, thicker initial SiGe layers and higher oxidation temperature can lead to larger relaxation rate and smaller defect density [5]. The successful operation of strained-SOI n-MOS, using this type of SGOI substrates has been achieved with the mobility enhancement of 1.67 under the Ge content of 23 % [6]. Also, 20-nm-order-strained-SOI structures with high Ge content (x>50%) has successfully been fabricated by the same method [7]

Using SGOI substrates made by the combination of SIMOX and oxidation [8], the operation of strained-SOI CMOS and CMOS ring oscillators have been demonstrated, for the first time [9]. Thin and thick strained-SOI substrates were used for fabricating FD and PD strained-SOI CMOS, as shown in Fig. 3. The mobility behaviors are shown in Fig. 4. The mobility enhancement of 1.85 and 1.53 has been obtained for n- and p-MOS, respectively, with strained-Si thickness of 25 nm and the Ge content of 25 %. It was also found from the waveform of 101-stage ring oscillators that strained-SOI CMOS is 70 % faster at V_{dd} of 1.5 V and 30 % faster at V_{dd} of 2.5 V than conventional SOI CMOS [9].

The author would like to thank M. Hirose, T. Kanayama, S. Kawamura, T. Masuhara, A. Toriumi, A. Kurobe, S. Watanabe and N. Fukushima for their continuous supports. This work was supported by NEDO.

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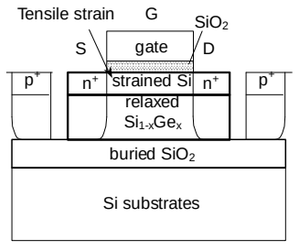

Fig. 1 Cross section of typical device structure of strained- SOI MOSFETs.

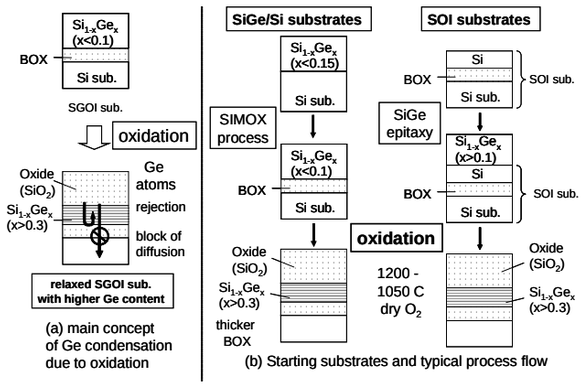

Fig. 2 (a) main concept of the fabrication technique to obtain SGOI substrates with high Ge content by oxidizing SGOI substrates with low Ge content, called Ge condensation technique (b) typical process flows using bulk Si and SOI substrates.

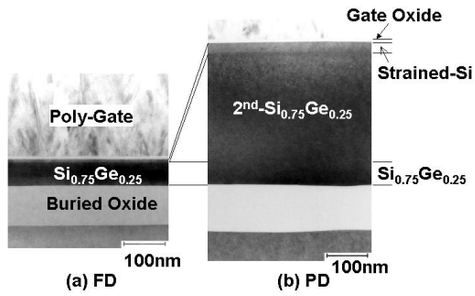

Fig. 3 TEM images of cross section of strained-SOI substrates, where CMOS was fabricated. Two types of substrates with different SiGe and strained-Si thickness ((a) 325nm/25nm (b) 53nm/7nm) were used for FD and PD-SOI MOSFETs, respectively.

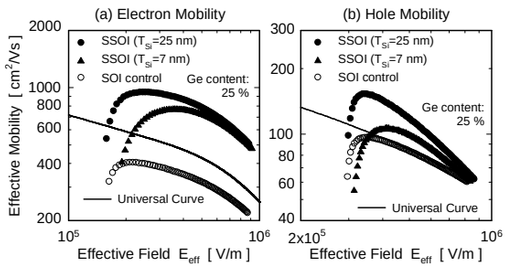

Fig. 4 Effective electron and hole mobility in strained-SOI CMOS as a function of E_{eff}. The universal mobility is also shown. Two types of substrates with strained-Si thickness of 25 and 7 nm were used for CMOS. The Ge content is 25 %.