Extremely Scaled FinFETs and Ultra-Thin Body SOI CMOS Devices

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We have performed extensive studies of both the FinFET double-gate (DG) device structure, as well as the single-gate, ultra-thin body (UTB) SOI MOSFET device structure. In both of these device structures, short channel effects are effectively controlled by using a thin silicon film, allowing for gate-length scaling down to the 10 nm regime [1]. In this presentation, we will review recent progress in the development of FinFET technology, including analysis of sensitivity to process variations, and show the results of circuit analysis of the benefits of FinFETs and UTB MOSFETs in terms of gate delay and energy consumption.

In order for a CMOS FinFET technology to provide maximum performance benefit over bulk-Si CMOS technology, various issues must be resolved. These include the formation of ultra-thin Si fins with high surface quality for high carrier mobilities, and the development of a tunable-work-function gate technology for threshold-voltage (V_t) control.

In an effort to improve the surface quality of the etched fin sidewall, we have investigated the use of pure hydrogen annealing after fin patterning. During the anneal in a pure hydrogen ambient, the surface (*vs.* bulk) silicon migration rate is enhanced [2]. Thus, line edge roughness caused by lithography and sidewall surface roughness caused by reactive-ion etching are reduced. Poly-Si-gated hydrogen-annealed FinFETs show higher on-state current and lower off-state current, as well as lower $|V_t|$ due to reduced trap density (Fig. 1). Low frequency noise measurements confirm the improvement in interface quality.

Ideally, the FinFET body should be lightly doped in order to achieve high carrier mobility for high transistor drive current, as well as immunity to dopant-fluctuation-induced variations in V_t. A major technological challenge, then, is V_t adjustment by gate work-function engineering. The required range of gate work functions for a fully-depleted CMOS FinFET technology is 4.4-5.0V [3], which precludes poly-Si as a gate material. Molybdenum (Mo) has a high work function (~5V), which makes it suitable as a gate material for p-channel FinFETs. We have previously shown that nitrogen implantation into Mo films followed by thermal annealing can be used to controllably lower the Mo gate work function to values as low as 4.4V [4], which is suitable for n-channel FinFET application. Here, we demonstrate the use of Mo gate technology for FinFETs. An example of V_t adjustment for p-FinFETs is shown in Fig. 2.

In order to properly explore a wide variety of trade-offs and make fair comparisons of device structures, we have done extensive circuit simulations. Device designs were based on ITRS roadmap specifications for high performance devices. An example of comparison of gate workfunction engineering approaches for bulk, UTB, and DG (FinFET) devices in terms of fan-out of 4 inverter delay is shown in Fig. 3. The use of a low-doped channel and metal gate with controlled work function shows the best performance due to the elimination of impurity scattering and reduced vertical electric field.
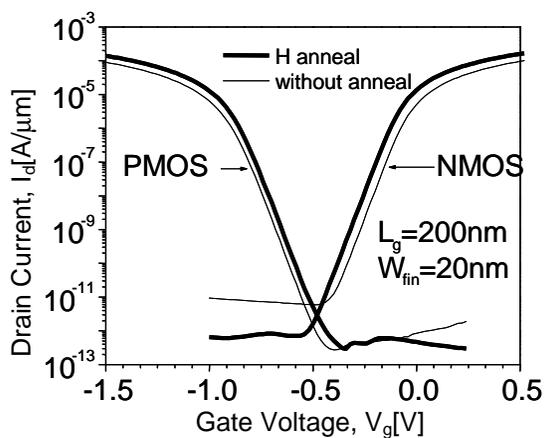

Fig. 1. I_d-V_g characteristics of FinFETs showing the effect of hydrogen annealing. Both NMOS and PMOS V_t are lowered, and drive currents increase.
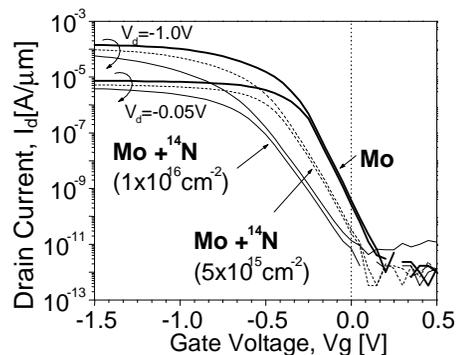

Fig. 2. I_d-V_g characteristics of Mo-gate FinFETs (L_g=80nm, W_{fin}=10nm). –0.2V V_t at 100nA/µm is achieved without body doping with pure PVD Mo-gate. Multiple V_ts are demonstrated by nitrogen implantation to change the gate work function.
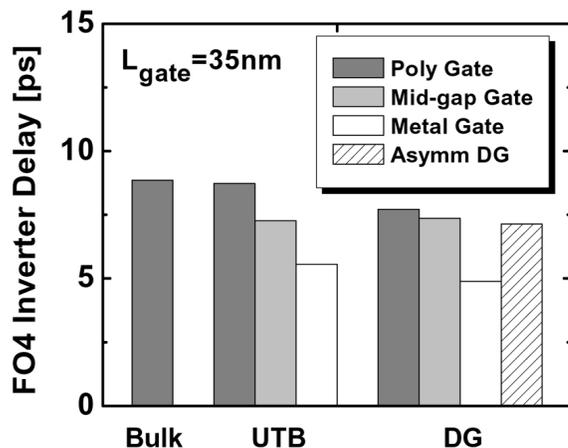

Fig. 3. Gate delay for a loaded (fan-out of four) inverter using various gate materials, and three device structures. For poly and mid-gap gate materials, channel doping is used to set threshold voltage. For metal gate and asymm DG cases, the channel is essentially undoped, and threshold voltage is set either by the gate workfunction of back-gate bias.

References

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