Status and Development of Future PD/SOI MOSFETs

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Partially Depleted SOI technologies are increasingly being implemented for use in high-performance CMOS applications [1]. This abstract describes current status and possible evolution of the PD/SOI MOSFETs.

High-performance applications (e.g., Microprocessors) need ever-improving MOSFET performance. However, as MOSFETs are scaled down into the sub-50nm regime, it is becoming increasingly difficult to meet the twin challenges of (a) improving performance, while (b) containing power dissipation. PD/SOI MOSFETs are good candidates for offering a better trade-off between power and performance. This is due to their low junction capacitance as well as potentially beneficial floating-body effects that can be exploited in circuit design. They are also relatively friendly to implement in a high-performance CMOS manufacturing environment. There are, however, key areas where special attention is needed.

In process integration, special attention needs to be given to isolation issues. It has been observed that the isolation process can significantly influence performance of the transistor. Specifically, the oxidation process used as a liner [2] after trench etch can cause stress in the SOI Islands. This can impact transistor and impact mobility and transistor drive current. Through process optimization, this can be suitably modulated and leveraged.

In device design, undesirable floating-body effects need to be contained. This includes DC and transient effects. Through appropriate lifetime killing methods [3], undesirable DC floating-body effects can be contained. AC effects such as hysteresis and parasitic BJT effects also need to be addressed to fully leverage SOI performance in circuits. Through junction capacitance optimization, we can modulate and control both hysteresis and parasitic BJT effects in floating body SOI. Examples of this will be discussed in the full manuscript.

Other needs for a robust SOI design & manufacturing will also be discussed (e.g., need for SOI models etc).

Future of PD/SOI and its derivatives will also be discussed in the full manuscript.

References:

1. G. Shahidi, “Mainstreaming SOI Technology”, IEEE International SOI Conference, pp. 1-4, 1999.
2. W. En, “Reduction of STI/active Stress on 0.18um SOI Devices through Modification of STI Process”, IEEE International SOI Conference, pp. 85-86, 2001.
3. T. Ohno et.al., “IEEE Transaction on Electron Devices”, pp. 1071-1076, 1998