Multi-Fin Double–Gate MOSFET Fabricated by Using (110)-Oriented SOI Wafers and Orientation-Dependent Etching.

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Double-gate MOSFETs (XMOSFETs) [1] have been regarded as the most promising candidate for ultimate MOSFET scaling [2] due to its excellent short-channel effect (SCE) immunity. Silicon-on-insulator (SOI) wafers have commonly been used in the fabrication of Fin-type double-gate MOSFETs (FinFETs) [3-5]. However, the cross-sectional shape of a Si-Fin reported so far looks like a trapezoid because reactive ion etching (RIE) has been used in the fabrication of the Si-Fins. Since the Si-Fin thickness affects the device parameters such as a threshold voltage, it is desirable to form the Si-Fin with a perfect rectangular cross-section especially for a multi-Fin double-gate MOSFET (MFXMOSFET) with high current drivability. In this paper, we report the MFXMOSFET with an ideal rectangular Si-Fin channel fabricated by using (110)-oriented SOI wafers and orientation-dependent etching.

Figure 1 shows the 3-D schematic diagram of the proposed MFXMOSFET structure. The fabrication processes of the MFXMOSFET are as follows. The starting material was the p-type (110) SOI wafer prepared by the epitaxial layer transfer technology (ELTRAN). The initial thicknesses of the SOI and buried oxide (BOX) layers were 100-nm and 300-nm. First, the wafers were thermally oxidized and multi-Fin EB-resist (SAL-601) patterns were formed by EB-lithography. The patterns were transferred to the SiO_2 layer on the SOI by RIE, and the SOI was etched with a 2.38% tetramethylammonium hydroxide (TMAH) solution at 50 °C for 1 min, to form nanoscale Si-Fins. Since the sidewall of the Si-Fin is the (111) plane with an extremely low etch rate compared with other planes, very narrow and straight Si-Fins can be fabricated by the orientation-dependent etching. After the gate oxide formation, the poly-Si gate was made by EB-lithography. Then, the n^+ doping for source-drain extension regions was performed by rapid thermal annealing (RTA), and finally aluminum electrodes were formed and sintered.

Figure 2 shows the cross-sectional SEM image of the fabricated MFXMOSFET with five-Fins. It should be noted that the widths at the top and bottom of the Si-Fin is entirely the same i.e., the Si-Fin shows the ideal rectangular channel shape. The measured I_d-V_d characteristics of the MFXMOSFETs with a single-Fin and five-Fins are shown in Figs. 3 and 4. It is apparent that 5 times of the drain current is accurately obtained in the five-Fin device compared with that of in the single-Fin device at a fixed gate voltage and drain voltage.

In summary, we have been succeeded in fabricating the MFXMOSFETs with an ideal rectangular Si-Fin cross-section, for the first time, by using (110) SOI wafers and orientation-dependent etching. The accurate current multiplication has experimentally been confirmed by the fabricated multi-Fin devices.

[1] T. Sekigawa et al.: Solid-State Electronics, 27 (1984) 827.
[2] H-S. Philip Wong et al.: Int. Electron Device Meet. Tech. Dig. (1997) 427.
[3] D. Hisamoto et al.: Int. Electron Device Meet. Tech. Dig. (1998) 1032.
[4] Y-K Choi etal.: Int. Electron Device Meet. Tech. Dig. (2001) 421.
[5] J. Kendzierski, et al.: Int. Electron Device Meet. Tech. Dig. (2001) 437.

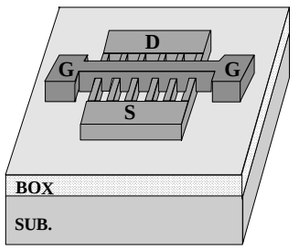

Fig. 1. 3-D schematic diagram of the proposed multi-Fin XMOSFET structure.

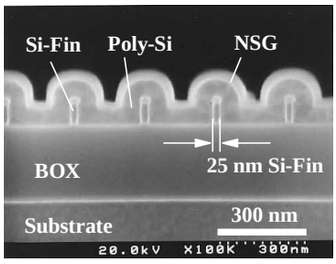

Fig. 2. Cross-sectional SEM image of the fabricated MFXMOSFET with 5-Fins.

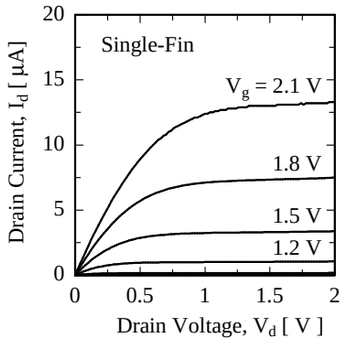

Fig. 3. I_d-V_d characteristics of the fabricated FXMOSFET with single-Fin.

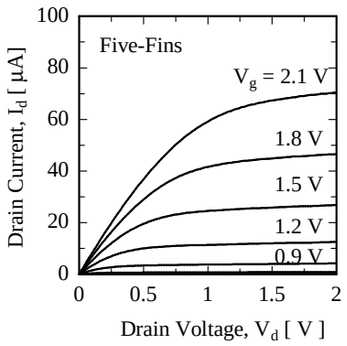

Fig. 4. I_d-V_d characteristics of the fabricated FXMOSFET with five-Fins.