OPTIMIZATION OF ULTRA-THIN BODY, FULLY-DEPLETED-SOI DEVICE, WITH RAISED SOURCE/DRAIN

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INTRODUCTION

We report on an ultra-thin body, fully depleted SOI device (FDSOI), with metal gate, raised source/drain, and its optimization via simulation. The physical gate length is 60 nm, the film thickness under the gate is 10 nm, and is undoped. The gate electrode is mid-gap, i.e., a workfunction of 4.6 eV. The source and drain regions are constant doping. The overlap region doping is Gaussian with a junction depth defined as the point at which the doping concentration drops to 10^{16} cm^{-3}, which for this device is 3 nm. Hydrodynamic simulations for capturing velocity overshoot are employed, with an energy relaxation time of 0.3 ps, and predicted I_{Dsat} is checked with Monte Carlo (1,2). Silicide resistivity is also included via a distributed resistance on S/D contacts (3), in both the continuum solver as well as Monte Carlo. The mobility model is from (4).

It is not sufficient to consider only I_{Dsat} for optimization of this device because of the possibility of much higher C_{GSD} with raised S/D (see Figure 1). CV/I is used as the criterion for optimization. Simulations include quantum effects via density-gradient (5) for the continuum solver, while Monte Carlo uses Schrodinger's equation for quantization.

In bulk, silicide is predicted to be 40% of the total resistance at the 50 nm physical gate length (6), and estimated to be 70-80% for very sharp junctions (7). The geometric parameters of this device are more sensitive to silicide resistivity because of the thinness of the silicon film. We will show the effects of the silicide resistivity on the performance of this device in terms of I_{Dsat} as well as CV/I. We also contrast the speed for epi deposition of the raised S/D before and after spacer deposition.

DISCUSSION

The results for the epi deposition for raising the source/drain before spacer formation are briefly summarized in Figure 2. In general, it can be said that the speed is dominated by the capacitance for this structure, most noticeably for the 5 nm liner case. In spite of the lower I_{Dsat} for the 10 nm epi (silicide reaches all the way to the buried oxide due to silicon consumption), this is the fastest device for a 5 nm liner and epi deposition before spacer formation. Surprisingly, the fastest device for either process sequence is the 60 nm epi after spacer with 2 x 10^{20} S/D doping (Figure 3). This is in spite of the fact that I_{Dsat} is 15% lower than for the equivalent device with epi before spacer. This again demonstrates the crucial role the added capacitive coupling plays in this raised S/D structure, and that I_{Dsat} should not be increased at all costs.

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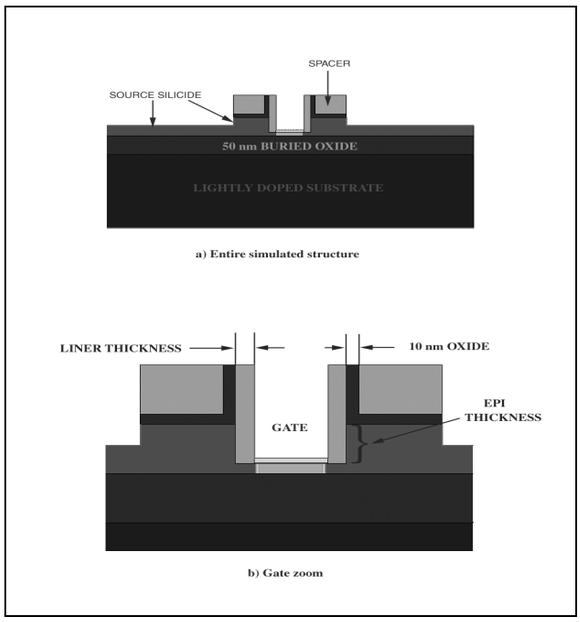

Figure 1: Simulated structure with definitions of relevant parameters.

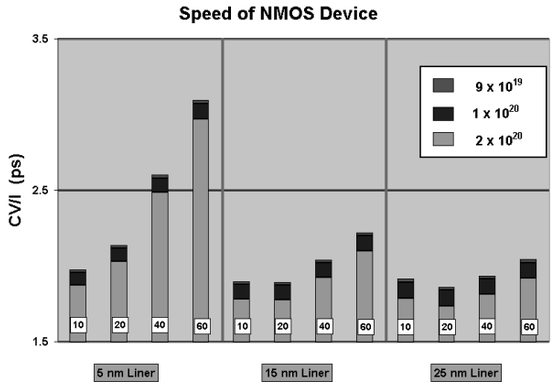

Figure 2: Speed of NMOS device for different epi and liner thicknesses, as well as S/D doping concentration, for the raised S/D epi depostion before spacer formation (as illustrated in Figure 1). There are 3 sets of data for liner thickness indicated at the bottom (5, 10, and 15 nm). Each set had epi thicknesses of 10, 20, 40, or 60 nm as indicated inside the bars. The S/D doping densities are indicated by color, as shown in the legend. This simulation included a distributed resistance of 2.4 x 10^{-8} Ω-cm^2, calculated from (3) for cobalt silicide. In general, it can be said that the speed of this structure is dominated by the capacitance.

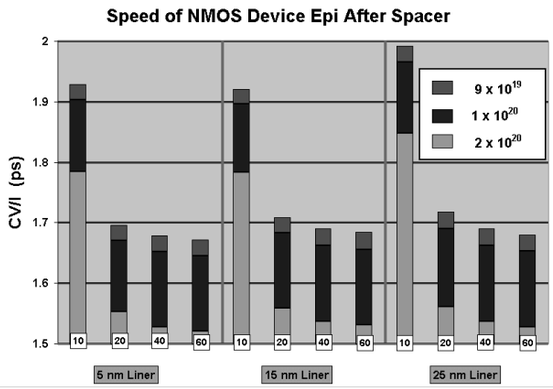

Figure 3: Speed of NMOS for the raised S/D epi deposition after spacer formation. Epi and liner thicknesses, as well as S/D doping concentration are indicated identically as in Figure 2. In contrast to the epi before spacer deposition, in general, it can be said that the speed for this structure is dominated by the saturation current. Note the different scales for Figures 2 and 3.