Partially Depleted SOI Dynamic Threshold MOSFET for low-voltage and microwave applications

M. Dehan, D. Vanhoenacker and J.-P. Raskin
Université catholique de Louvain, Microwave Lab.
Place du Levant, 3, 1348 Louvain-la-Neuve, Belgium
E-mail: dehan@emic.ucl.ac.be

Introduction

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Silicon-on-Insulator (SOI) based MOSFET's are very promising devices for multigigahertz applications. SOI MOSFET's offer indeed interesting low-voltage performances, higher speed and increased integration density, all with simpler processing than bulk silicon MOSFETs of comparable size [1]. In order to reduce the power consumption and keeping good RF performances, we present in this paper new results of sub-micron Dynamic Threshold (DT) MOSFET [2] designed on a standard Partially Depleted (PD) SOI technology.

Device Fabrication

DTMOS is a MOS transistor for which the gate and the body channel are tied together. Figure 1 shows the 3-D structure for conventional and DT MOSFETs. Any variations of the gate potential induce the same variations to the body, dynamically changing the threshold voltage (V_{th}). As a consequence, the effective V_{th} is reduced as well as the inverse of the subthreshold slope and the body effect. The main advantage of DTMOS over conventional MOS is its higher drive current at low bias conditions. To keep the body to source current as low as possible, the body bias voltage must be kept lower than 0.7 V. DT MOSFETs were composed of 12 fingers with a gate length of 0.25 µm. The gate was connected to the floating body of the transistor from both sides of the gate fingers. The width of each finger was as small as 3.3 µm in order to ensure a good control of potential distribution of the body throughout the entire transistor width. The transistors were embedded in a coplanar waveguide (CPW) structure in order to be correctly measured on-wafer from 40 MHz up to 40 GHz using a Vector Network Analyzer.

Experimental results

After measuring on-wafer the S-parameters of transistors, two successive calibrations have been used to bring back the measurement reference planes at the edges of the device active area; one commercially available Alumina calibration kit and one home made calibration test set built on SOI wafer close the devices to be characterized. From the S-parameters measurements small-signal equivalent circuits have been extracted using characterization techniques described in [3] in order to fairly compared the RF performances of various SOI PD conventional MOS and DTMOS. Table 1 shows that thanks to the dynamic threshold effect, under lower DC bias, much higher gate transconductance are obtained with DTMOS compared to the one from the conventional MOSFET (Fig. 2), but DTMOS exhibit also a higher total gate capacitance due to its more complex 3-D interconnect structure. It results that the cut-off frequency is nearly the same for both devices. On the other hand, we did not observe any strong influence of the non infinite input resistance of DTMOS on the RF characteristics. Therefore, the gate-to-body impedance is transparent at RF as long as the DTMOS properly works keeping the parasitic bipolar transistor off (i.e. $V_g < 0.7$ V).

Conclusion

These RF results demonstrate, for the first time, the interest of DTMOS structure for reaching the best RF performances of a PD SOI technology node under lower DC bias conditions. More experimental results will be shown at the conference for 80 nm PD SOI DTMOS technology as well as RF noise and non-linear characteristics.

References

[1] J.-P. Colinge, "Silicon-on-Insulator technology: material to VLSI", KAP Publishers, 1991.
[2] F. Assaderaghi *et al.*, *IEEE Trans. on Electronic Devices*, vol. 44, no. 3, pp. 414-422, 1997.
[3] J.-P. Raskin *et al.*, *IEEE Trans. on Electron Devices*, vol. 45, no. 5, pp. 1017-1025, May 1998.

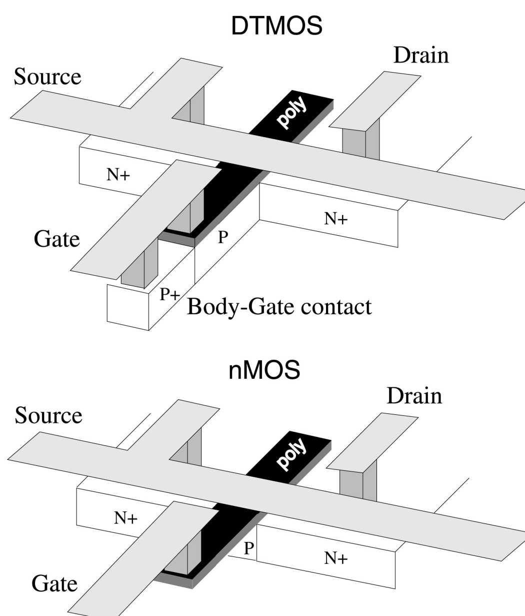

Fig. 1. 3-D structures of SOI DTMOS and nMOS.

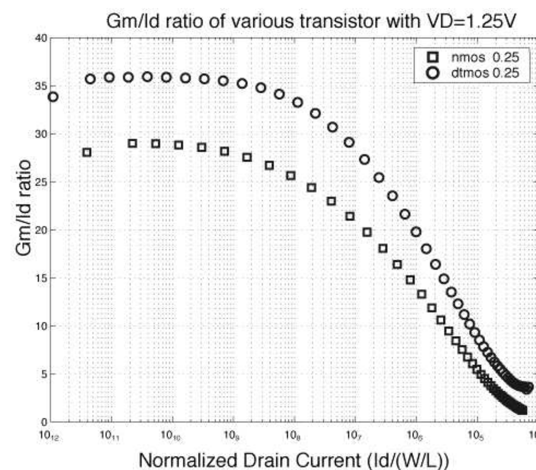

Fig. 2. Measured G_m/I_d ratios vs. normalized current for PD SOI MOSFET and DTMOS.

	PD SOI nMOS	PD SOI DTMOS
V_g	1	0.7
V_d	1.5	1.5
F_t *(GHz)*	38	36
G_m *(mS)*	11.5	20
C_{gg} *(fF)*	46.5	92

Table 1. Extracted small signal parameters of conventional and DT SOI PD MOS.