Intra-die temperature non uniformity related to front side emissivity dependance during Rapid Thermal Annealing

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Using Rapid Thermal Processing (RTP) to achieve Ultra Shallow Junction (USJ) is the best-known solution for CMOS devices down to 100 nm node [1]. Annealing with lamp-based system is a widely used technique for this application. Due to the use of very low energy implant, the USJ characteristics exhibit increased temperature sensitivity. Any temperature variation will results in enhanced junction non-uniformity. For the lamp-based systems, the emissivity effects are known to be a serious issue for temperature control. Regarding the emissivity of wafer backside, the problems have been solved by using tools with emissivity measurements and correction loop. However, the emissivity variation within the wafer or even within a die (due to different materials or patterns) is a still an issue. Indeed, previous works have clearly shown that front side different materials resulted in emissivity variations that can lead to a significant local variation of the temperature [2-4]. Junction sheet-resistance variation as high as 25%, due to emissivity variation has been reported [4]. This sheet resistance variation has been measured between the centre and the edge of 18 mm-wide die using four-point probe technique. The spatial resolution of this technique is not high enough to allow accurate profiling of the sheet resistance within a single die.

In this article, we will present further characterization results based on SIMS and Van der Pauw measurements and also oxide thickness measurements

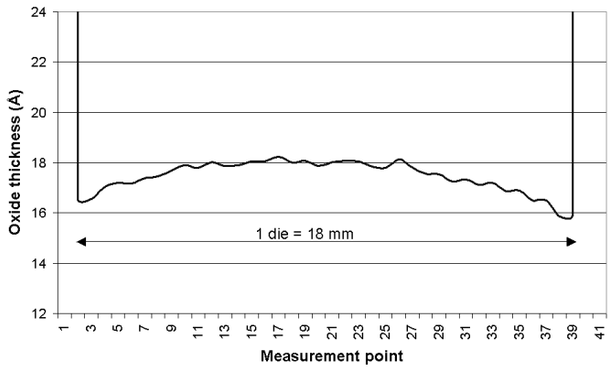

Figure 1 : oxide thickness intra die variation after RTO on lamp based system, on a patterned wafer with different emissivity materials.

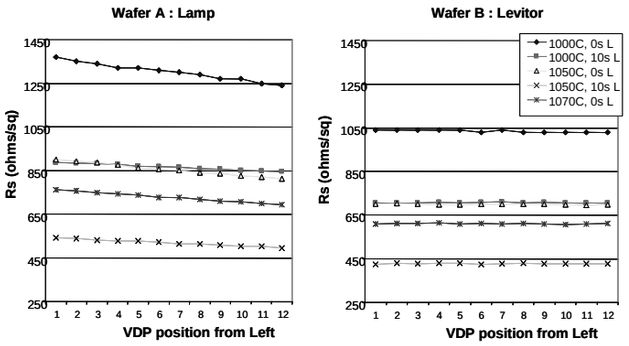

Figure 2 : Van der Pauw measurement compared between wafer A processed on a lamp based system and wafer B processed on a Levitor system, with different temperatures and time processes.

within a die after Rapid Thermal Oxidation on a lamp-based system..

From SIMS measurements, we will show that for 500 eV boron-implant, 10°C temperature variation resulted in 15% change in the junction depth. However for higher energy implant (5 keV boron) the junction is less sensitive to the temperature variation and we observed a slight junction depth variation within a die.

Rapid Thermal Oxidation on the lamp based system shows (Fig. 1) how a large feature with different emissivity material (in that case, $\Delta\varepsilon = 0.3$) impacts intra die temperature and oxide thickness. As the oxide thickness measurement spot size is small, those values are significant until the pattern edge.

Smaller features such as Van der Pauw structures that are also more consistent with devices features were processed (Fig.2). Polysilicon features were patterned on oxide and implanted with N-type or P-type dopant. Wafer annealed with lamps clearly shows a sheet resistance variation along the line, when this effect seems to be negligible on the Levitor annealing tool, which is mainly based on conduction heat transfer, and as such is not sensitive to emissivity variations.

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