Pattern Effects During Spike Annealing of Ultra Shallow Implants

J. Niess, Z. Nényei, W. Lerch, S. Paul
Mattson Thermal Products GmbH
Daimlerstrasse 10, 89160 Dornstadt, Germany

Hotshielding technology is a proven method for pattern effect reduction in halogen lamp based rapid thermal annealing (RTA) systems. Is the requirement for sharpest spikes for ultra shallow junction (USJ) activation in contradiction with this method? It seems that photon effects can have an impact on the activation/diffusion balance and can at least partly dissolve this trade-off.

Pattern effects during RTA have been increasingly observed during the last few years. The general trends in IC production include the use of larger die-sizes, complex intra-dies structures associated with system-on-chip designs and non-patterned peripheries, and all of which can have a profound influence on pattern-related thermal and process non-uniformities during RTA [1,2].

In halogen lamp based RTP systems the Hot Shielding technology is proven to strongly reduce such pattern effects [3,4]. The Hot Shield is a second wafer above the product wafer which protects the front side of the latter against the incoming direct radiant flux from the heating source. A potential drawback of this technology is the doubling of the thermal mass to be heated. While in standard RTP applications the available power is still high enough to maintain required ramp rates it might be expected that there would be a problem for spike anneals. For these processes very high ramp rates, fast turn-around speeds and fast cooling are all desirable [5,6]. However the loading effects of different patterns and resulting pattern-induced non-uniformities are expected to pose serious challenges for spike annealing.

Despite the apparent incompatibility of the Hot Shielding technology with spike-anneal processing, this paper shows that the sheet resistance, $R_{S,}$ versus junction depth, X_J, data from spike anneals with a Hot Shield are comparable to USJ results obtained without the Hot Shield. The data were obtained from a Mattson 3000 RTP tool with ramp rates of 150 K/s on 200 mm wafers..

Fig. 1 shows the comparison of two SIMS profiles of an annealed $^{11}B^+$, 500eV, 1E15 cm^{-2} implant. One is taken after standard spike annealing without Hot Shield, the other one is after spike annealing with a Hot Shield. Ramp rates in both cases were set to 150 K/s. With Hot Shield a broader spike width of 2.23 s at (T_{peak} - 50 K) was observed compared to 1.9 s without Hot Shield. The peak temperature was reduced from 1044 °C without Hot Shield down to 1039 °C with Hot Shield to maintain an identical R_S of both samples (486 Ω/sq.).

A possible explanation of the well comparable or even slightly reduced junction depth after Hot Shield annealing could be a reduced high energy photon flux to the implanted front side of the wafer compared to a standard spike anneal without Hot Shield. The conclusion therefore would be that a high energy photon flux as applied for spike annealing could enhance boron diffusivity of ultra shallow implants. This would then also be in accordance to the results of Jung and Seebauer [7] who showed that nonthermal illumination can enhance (or reduce) Si self diffusion.

REFERENCES

1. R. Berger, S. Miethaner, H. Gruber, J. Niess, W. Dietl, Z. Nényei: "Pattern Shift Reduction in Dual Side Heated RTP Systems with Hot Shielding Technology." *RTP´01 Conference Proc., Anchorage Ak* (2001), 71-77.
2. J. Niess, R. Berger, P.J. Timans, Z. Nényei: "Pattern Effects and how to Explore them." *RTP´02 Conference Proc., Vancouver Canada* (2002), 49-57.
3. L.H. Nguyen, W. Dietl, J. Niess, Z. Nényei, S.P. Tay, G. Obermeier, D.F. Downey: "Logic in RTP." *RTP´99 Conference Proc., Colorado Springs, CO* (1999), 26-38.
4. Z. Nényei, J. Niess, S. Buschbaum, K. Meyer, W. Dietl, R. Berger, S. Miethaner, H. Gruber, R. Wahlich, S. Chamberlain: "Pattern Effects in RTP: Still a Hidden World in Production?" *Rapid Thermal and Other Short-Time Processing Technologies III, Electrochemical Society Proceedings* 2002, to be printed.
5. W. Lerch, B. Bayha, D.F. Downey, E.A. Arevalo: "State of the Art Techniques for Ultra-Shallow Junction Formation." *Rapid Thermal and Other Short-Time Processing Technologies II, Electrochemical Society Proceedings* **2001-9**, 312-336
6. S. Paul, B. Bayha, W. Lerch, C. Merkl, D.F. Downey, E.A. Arevalo: "Production Worthy Repeatability of Spike Anneals." IIT2002 conference, Taos, New Mexico. Presented and accepted for publication.
7. M.Y.L. Jung, E.G. Seebauer: "Measurement of Nonthermal Illumination-Enhanced Diffusion in Silicon." *RTP´02 Conference Proc., Vancouver Canada* (2002), 133-135.

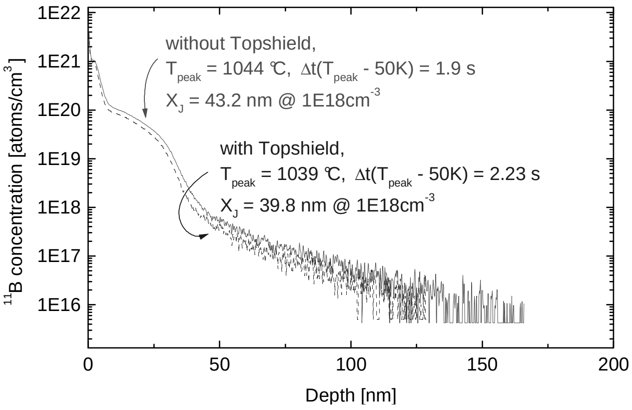

fig. 1: SIMS profiles after implant activation of a $^{11}B^+$, 500eV, 1E15 cm^{-2} implant by spike annealing with 150K/s ramp up rate without (solid line) and with Hot Shield (dashed line), both resulting in $R_S \approx 486$ Ω/sq.