Junction Scaling Technology for the Sub 90nm Node

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Since the inception of the semiconductor industry, the advances predicted by Moore's law have remained uninterrupted. Recent advances in process tools like RTP spike anneal and the electron volt implant have enabled the required junction scaling. However, these advances do not occur every process generation. In the alternate generations, scaling relies on process innovations to maximize the benefits to be derived from these technologies. Extending junction technology beyond the 90 nm technology node will be examined.

Two approaches to junction scaling will be examined. The effects of incremental increses in RTP ramp rates in a spike anneal process and co-doping effects. Figure 1 shows the effect of RTP ramp up/down rates on the junction depth. This simulation shows that unless there are significant improvements to the cool down rates, the junction scaling benefits are limited. Figure 2 shows a SIMS plot of a deep boron implant. Co-implantation with Germanium significantly reduces the diffusion tail but does not negatively impact the junction sheet resistance. This impact is greater than can be achieved with a realistic increase in the RTP ramp rates.

A fundamental understanding of the dopant anneal, diffusion and activation mechanisms is necessary to engineer the optimal transistor junction. This presentation will cover transistor scaling, dopant-defect interactions, the impact of annealing and implant process conditions and will be accompanied with modeling studies.

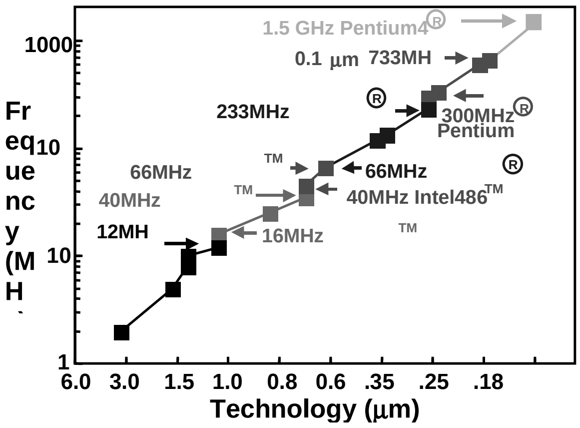
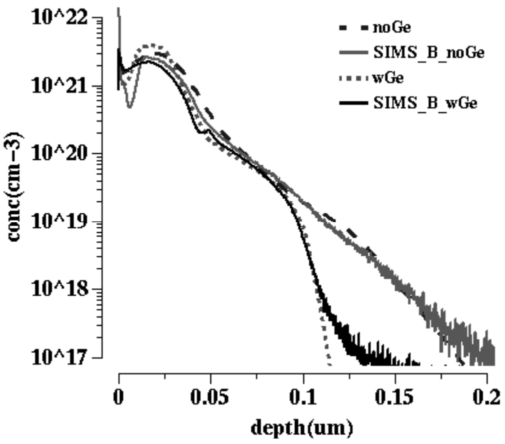


Figure 1. Moore's law remains uninterrupted.

Figure 2. Junction depth vs. RTP ramp up/down. Improving junction Rs vs. junction depth requires a faster RTP cooldown.



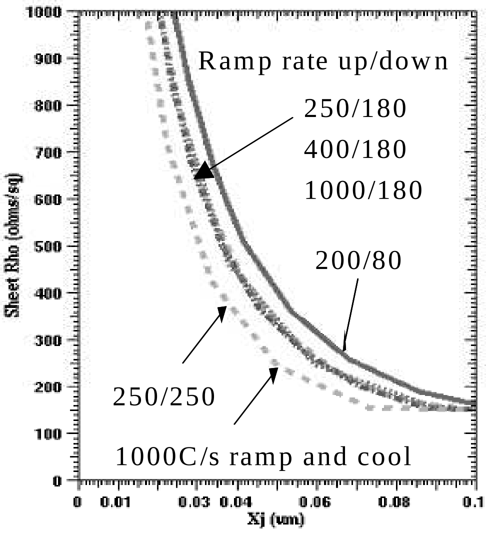


Figure 3. Use of germanium as a co-implant significantly reduces the boron diffusion tail without a significant reduction in sheet resistance (Hal Kennel et al., IEDM 2002).

References

Hal Kennel et. al, IEDM 2002.