The Role of F with Ge Pre-Amorphisation in Forming pMOS Junctions for the 65 nm CMOS technology node.

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The limits of using B or BF_2 alone in forming ultra-shallow junctions have been reached for the 90nm CMOS generation. In this paper we evaluate the use of Ge and F co-implants to extend conventional implantation and spike anneal to the 65nm CMOS technology node.

In this work, we investigate the effect of the Ge and F profile and crystalline regrowth rate on B activation and diffusion. The results indicate increased B diffusion in amorphous Si in the presence of F. This is contrary to single-crystal Si where F is seen to reduce transient enhanced diffusion (TED). By positioning the amorphous depth and F implant correctly, a more box-like junction profile can be obtained. Results show that by increasing the spike ramp up at the regrowth temperatures, the dopant diffusion can be minimized in both the amorphous and single crystal Si while preventing B clustering in the near-surface region.

Results also show a clear dependence of B activation on the F dose in the amorphous Si. Doses less than 1e15ions/cm^2 produce a junction with higher resistance due to limited B diffusion in the amorphous Si, whereas doses greater than 1e15ions/cm^2 begin to reduce the B activation level. The optimum F dose is than 1e15ions/ cm^2. We show that the optimized Ge, F and B implant is also dependent on the spike anneal temperature and the ramp up. For these co-implantation conditions the fast temperature ramp-up B activation in sub-30nm junctions produces junction depth reduction up to 10nm for the same sheet resistance.

The best combination is shown to be with a 35nm deep pre-amorphization by Ge, a F co-implantation positioned deep in the amorphous region, followed by B doping and spike annealed at 1070°C for 0s and ramp-up rate of 800^{o}C/s. With these conditions a junction abruptness of 4.5nm/decade is obtained with a junction depth below 27nm and sheet resistance less than 700Ohm/sq.