RAPID THERMAL PROCESSING IN SILICON: MICROELECTRONICS TO SOLAR CELLS

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Rapid thermal processing (RTP) has been very successfully applied in the microelectronics industry. This has particular relevance for complementary metal oxide semiconductor (CMOS) technology, for process steps such as implant annealing, oxidation, source and drain contact junctions, shallow-extension junctions between the channel and the contacts, and electrically active polycrystalline-silicon gate electrodes.[1,2] For very large scale integration (VLSI) circuit processing, RTP has evolved from low-ramp-rate/high-temperature for a short time to high-ramp-rate/high-temperature for ≈ zero second (spike) anneals. These considerations necessitate that RTP systems be capable of very high power-density illumination, active cooling, and thermal compensation for edge-radiation losses of the process wafer. With the advent of 300-mm-diameter, double-side polished wafers in the silicon integrated-circuit (IC) industry, the problems relating to temperature nonuniformity across the wafer seem to have been minimized. However, local temperature variations can occur because of the variable emissivity across the IC patterns on the wafer.[3] In spite of the International Technology Roadmap for Semiconductors (ITRS)[4] forecasting disruptive changes in future process technologies, rapid thermal annealing (RTA) appears to be viable to at least the 60-nm node.[5] RTA (and ion-implantation) is indeed being used and implemented successfully for the current 90–130 nm technologies.[2] With the current trend of increased interest in non-planar CMOS devices, belt-type RTP systems offer advantages of reduced cost and increased throughput.

Recently, RTP-like processing has found applications in another rapidly growing field — solar cell fabrication. RTP-like processing, in which an increase in the temperature of the semiconductor sample is produced by the absorption of the optical flux, is now used for a host of solar cell fabrication steps, including phosphorus diffusion for N/P junction formation and impurity gettering, hydrogen diffusion for impurity and defect passivation, and formation of screen-printed contacts using Ag-ink for the front and Al-ink for back contacts, respectively. The demands on an RTP system for solar cell fabrication are quite different from those for traditional microelectronics applications. Here, the primary emphasis is on throughput and cost (cost of ownership). These major considerations have resulted in RTP systems being belt-type, IR systems, which use tungsten-halogen lamps to illuminate the wafers from one side. The need for low-cost equipment and high throughput (600 wafers/hr) has some ramifications for process uniformity, with concomitant implications for the device performance. Process nonuniformities in solar cell fabrication arise from several sources:

1. Commercial Si solar cells use low-cost, multi-crystalline wafers. These wafers are chemically textured to minimize surface reflectance. However, because texturing is orientation dependent, grains of different orientations have different reflectance and light-scattering properties, resulting in variations in emissivity from grain to grain. Thus, even for blanket diffusions for formation of an N+ junction in an un-patterned wafer, the RTP process can have spatial temperature variations.
2. In a patterned wafer (e.g., metallization anneal) there can be thermal nonuniformities introduced by large pattern dimensions. Solar cell metallization has typically 75–100-μm grid lines and 1mm bus bars. Furthermore, screen printed metal is 25–50-μm thick. Thermal mass and optical shadowing causes large lateral variations in the temperature.

Thus, one of the common problems in the RTP of Si devices arises due to local variations in the emissivity of the wafer. These variations can greatly influence solar cell performance.

This paper will focus on RTP application for metallization annealing. Metallization anneal is a multifunction process step. A typical metallization process consists of:
Deposition of about 750 Å of a SiN film by a PECVD process on the front side of the solar cell. During this process, some H is introduced in Si that resides near the surface. Next, metallization patterns are screen printed on the front and the backsides of the cell using Ag and Al pastes, respectively. Then, the cell is rapidly annealed in an IR furnace, whereby metallization contact is fired through the nitride and the back contact is alloyed. In addition, H diffuses into the bulk of the device.

It is clear that the role of nitride is quite complex, and a control of optical and electronic properties of the device requires a detailed knowledge of various mechanisms that influence optical parameters, interface charge, and transport of H.[6,7] In this paper, we will present our current understanding of these mechanisms and describe a systematic process sequence for optimization of solar cell performance. In a multifunction process such as this, temperature nonuniformities can have a strong influence on the device performance. We will discuss the various emissivity models and compensating schemes to minimize the effects of temperature non-uniformity across the wafer.

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