SIDEWALL GROOVING ON $COSI_2$ NARROW LINES

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Today, cobalt silicide is a preferred material for contacts on both source-drain areas and poly-Si interconnects in CMOS fabrication. The low resistivity of $CoSi_2$, its good thermal stability and no resistivity degradation on narrow lines are the main reasons for use of $CoSi_2$ in a self-aligned-silicide (SALICIDE) process (1). However, thin silicide films on active regions, needed for ultra-shallow junctions, agglomerate at elevated temperatures to minimize the energy of the silicide/silicon system (2). Moreover, when the silicide is formed on very narrow lines, morphology and thermo-stability of the silicide can be affected by lateral confinement (3). Particularly, we observed voids, or sidewall grooving, in the silicide along the isolation edges on narrow active lines with $CoSi_2$ formed from Co/Ti layers (Fig.1).

In this work, the appearance of these sidewall-grooving defects in silicide lines on monocrystalline Si was studied. The effects of doping, stress, surface pre-clean, substrate crystallinity, and anneal temperature, were investigated by optical inspection, Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM) and sheet resistance measurements.

To identify the main factors causing the defects, a number of silicidation parameters were varied. These included dopants type, isolation, preclean, preamorphisation of Si substrate, deposition conditions, silicide thickness, and anneal conditions.

We found that sidewall grooving occurs at the grain boundaries of $CoSi_2$ (Fig.2) and its origin is in the formation of Co-disilicide phase on c-Si. Some parameters seem to have no (or little) effect on sidewall grooving, e.g. silicide thickness, stress, surface conditions and RTP conditions. On the other hand, linewidth and type of doping are crucial for void formation. Firstly, the number of defects increases with decreasing linewidth – a bamboo-like structure is formed when linewidth is comparable to the Co-silicide grain size (app.200 nm). Secondly, the problem is most pronounced on As-doped silicon (it is also present on As with P-coimplantation and on BF_2-doped substrates). Another important factor is the crystallinity of the Si: sidewall grooving was not observed on a-Si (Fig.3). As the linewidth, doping, and substrate crystallinity are parameters affecting the silicide grain size, we conclude that sidewall grooving is caused by minimization of $CoSi_2$ surface energy and grain boundary energy when the surface/volume ratio increases.

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Figure 1. Plan-view SEM picture of a silicided active line. Sidewall grooving defects are indicated by arrows.

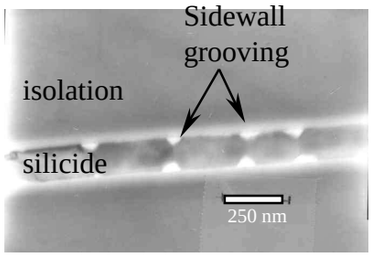

Figure 2. Plan-view TEM image of a narrow line: $CoSi_2$ grains form a bamboo-like structure.

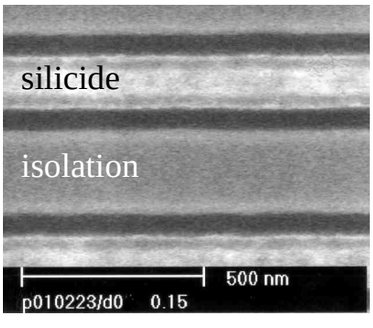

Figure 3. Plan-view SEM of CoSi2 lines formed on a-Si. No sidewall grooving is observed.