Metal Interconnect Technologies for CMOS ULSI

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1. Introduction

According to the scaling rule, it is necessary to reduce device feature sizes for improving CMOS performance. In order to improve current driving capability of the scaled CMOS for high-speed operation, low-resistance silicide technologies such as titanium silicide, cobalt silicide and nickel silicide have been developed. Furthermore, low-resistivity copper interconnects in conjunction with low-k interlayer dielectrics have been developed to improve RC delay time in scaled global interconnects.

In this paper metal interconnect technologies such as salicide and Cu interconnects are described in terms of high-speed performance of ULSI.

2. Salicide

$TiSi_2$ has been used for several technology nodes down to 0.25 μm, but it has become difficult to use for sub 0.25 μm technologies due to the difficulty of maintaining low sheet resistance on small geometries. $TiSi_2$ has phase transformation from the high resistivity C49 to the low resistivity C54. Nucleation and growth of the high resistivity C49 $TiSi_2$ have been observed to precede nucleation of C54 $TiSi_2$. A salicide formation anneal is carried out by use of rapid thermal processing to convert the $TiSi_2$ from C49 to C54. In order to suppress line width dependence, a significant improvement was achieved with pre-amorphization implantation of arsenic atoms and high temperature sputtering of Ti.[1] Arsenic ion implantation was carried out for Si amorphization in source, drain and gate. Ti was deposited on the pre-amorphized Si substrate and poly-Si by DC magnetron sputtering at 450C. The first RTP was carried out at 650C, and then non-reacted silicide layer was removed by wet chemicals. The second RTP was carried out at 750C. As a result, the line-width dependence of $TiSi_2$ was suppressed down to 0.15 μm and the difference of sheet resistances in p-type and n-type Si was eliminated.

$CoSi_2$ has been introduced as an alternative to $TiSi_2$ for 0.18 and 0.13 μm technology nodes because $CoSi_2$ does not have the line width effect as $TiSi_2$ but it is more sensitive to junction depth as well as Si surface conditions. As a consequence, additional Ti deposition is necessary to reduce native oxide on Si. Ti and Co co-depositions and Ti or TiN capping layer deposition were necessary to solve this problem. High temperature sputtering of Co and in-situ vacuum annealing have been developed for $CoSi_2$ formation without additional Ti deposition.[2] No line width dependence of sheet resistance was observed down to 100 nm. The sheet resistance of 11Ω/□ for both gate electrode and diffusion layer was obtained with 5 nm thick Co. Furthermore, high temperature sputtering led to the growth of epitaxial $CoSi_2$ with high thermal stability.

It is expected that NiSi will be introduced to sub-100 nm technology nodes because of its low thermal budget for processing. The low sheet resistance was obtained for both p- and n-type Si substrates in the wide process temperature range from 500 to 750C. No line width dependence was observed.

3. Cu Interconnect

Cu interconnects have been introduced to for CMOS ULSI to substitute Al because of its lower resistivity and higher electromigration resistance. However, Cu could not be patterned by conventional halogen plasma etching process because of the low vapor pressure of its compound. Consequently chemical mechanical polishing process was introduced for patterning Cu lines. Cu is deposited by electroplating on Cu seed layer in trench lines formed in interlayer dielectric films. Dual damascene process was developed to reduce process steps for Cu via and line formation for multilevel interconnects.

In order to improve high-frequency performance of CMOS ULSI, it is necessary to reduce not only resistivity of metal interconnects but also capacitance of interlayer dielectrics. Porous low-k interlayer dielectrics are needed to reduce dielectric constants less than 2.0 for future CMOS. However, the mechanical strength decreased with increasing porosity. Consequently, it is necessary to develop ultra-low-k films with both sufficient elastic modulus and lower dielectric constant.

4. Summary

Low-resistivity salicides for transistors and low-resistivity metal interconnects with low-k dielectrics for global interconnects are key technologies for future CMOS ULSI.

References

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[2] K. Inoue, K. Mikagi, S. Chikaki, and T. Kikkawa, IEEE Trans on Electron. Devices, vol.45, No.11, pp. 2312-2318, 1998.