Study on Ge/Si ratio and formation of Ni/ $P^+Si_{1-x}Ge_x$ and Ni/Si/$P^+Si_{1-x}Ge_x$

Tsung-Hsi Yang, Edward Yi Chang[a)], Tsung-Yea Yang[b)], Hua-Chou Tseng[c)], Han-Yu Chen[d)], Chun-Yen Chang[a, d)]

[a)] Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C

[b)] Department of Materials Engineering, Tatung University, 104 Taipei, Taiwan, R.O.C

[c)] United Microelectronics Corporation, Hsinchu, Taiwan, R.O.C

[d)] Department of Electrons Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C

As the transistor continue to scale down, the characteristics of $Ni/Si_{1-x}Ge_x$ and $Ni/Si/Si_{1-x}Ge_x$ junction have received lots of attention because of its potential applications to heterojunction bipolar transistors. In this study, we have fabricated Ni silicide on 35 nm-Si/$P^+Si_{1-x}Ge_x$ and Ni germano-silicide on $P^+Si_{1-x}Ge_x$. The Ni silicide shows a low sheet resistance of 4.75-5.75Ω/□ on 35 nm Si consuming layer, which is smaller than Ni germano-silicide on $P^+Si_{1-x}Ge_x$ (6.85-7.57Ω/□) at a RTA temperature of 450-550℃ for 30 s are shown in Fig.1.

For improving excellent sheet resistance of the silicide film, an appropriately thickness of the Si consuming layer should be adopted. Figure 2 shows the sheet resistance ρ_S as a function of Ge mole fraction after annealing at 500℃ for 30 s by RTA. The ρ_S value of the no Si consuming layer-annealed samples is larger than that of Si consuming layer-annealed counterparts. In addition, the small mean roughness, no surface Ni accumulation and no surface Ge agglomeration are obtained for 35 nm Si consuming layer at RTA temperature 500℃ for 30 s are shown in Fig.3, that are the reasons to achieve such low sheet resistance.

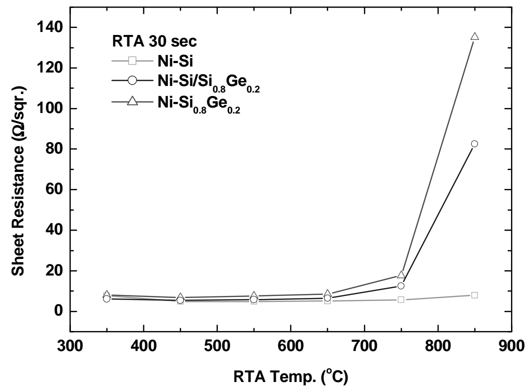

Fig. 1. Sheet resistance comparison of Ni silicide and Ni germano-silicide on Ni/PSi, Ni/Si/$P^+Si_{1-x}Ge_x$ and Ni/$P^+Si_{1-x}Ge_x$ samples.

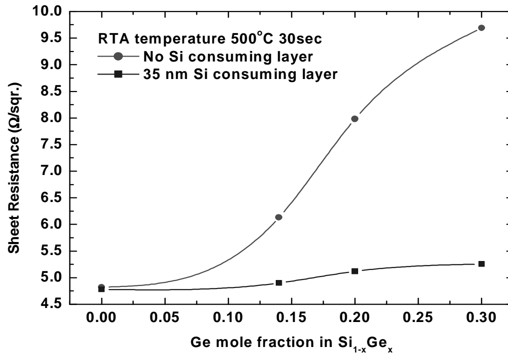

Fig. 2. Sheet resistance as a function of Ge mole fraction for 35 nm Si consuming layer and no Si consuming layer after annealing at 500℃ for 30 s.

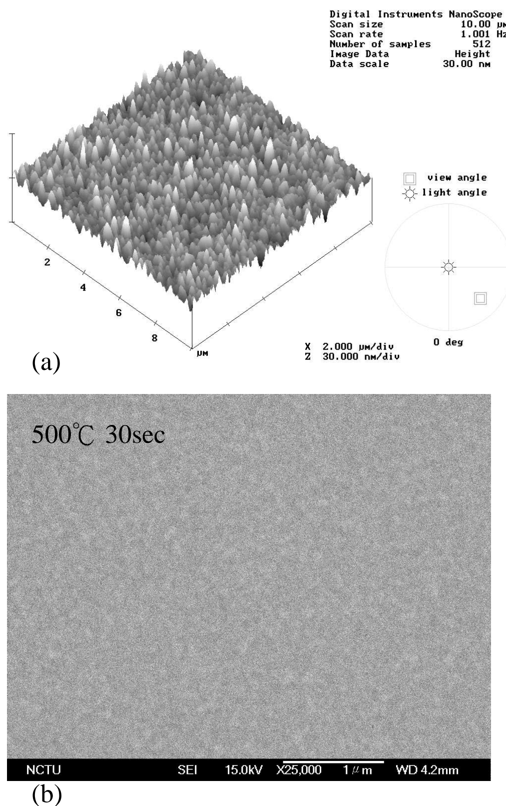

Fig. 3. (a) The AFM image shows the mean roughness of 35 nm Si consuming layer is 1.398nm (b) The SEM image shows no surface Ni accumulation and no surface Ge agglomeration are obtained for 35 nm Si consuming layer