APPLICATION OF HIGH K DIELECTRICS IN CMOS TECHNOLOGY AND EMERGING NEW TECHNOLOGY

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The maturing of high permittivity dielectric materials marks probably the most important progress in CMOS technology in the last decade. In this paper we will review three critical applications that not only allow continued scaling of CMOS logic and memory devices, but also open up new technology opportunities for more powerful System-on-Chip (SoC) devices.

High K gate dielectric

Below 90nm technology node gate leakage by tunneling becomes intolerably high if current SiO_2 based dielectric is used. In addition, n- and p-type doped polysilicon gate is used for CMOS devices and B in p-type polysilicon diffuses into and through thin gate oxide, severely degrades pFET performance. Replacing SiO_2 with a somewhat thicker high K dielectric will allow the achieving of tox (equivalent oxide thickness) of < 1nm, and thus will allow further scaling of MOS devices below 90nm node.

High permittivity dielectric such as ZrO_2 and HfO_2 deposited by various techniques, PVD, CVD and ALD, have demonstrated capabilities to reduce gate leakage by more than one order of magnitude [1]. However, severe carrier mobility degradation is also observed. The mobility degradation may be caused by traps at the dielectric/Si interface. Growing a SiO_2 oxide before high K dielectric deposition improved mobility somewhat, but also takes away precious tox. In addition, it is also found that high K dielectric does not prevent B penetration into Si substrate and nitrogen needs to be incorporated to control pFET threshold voltage. Finally, high K dielectrics obtained so far have all shown considerable fixed charge within the dielectric. This degrades both the subthreshold slope of the MOS device and the reliability of the dielectric.

Despite the above issues, however, high K dielectric remains the only viable hope for continued scaling for CMOS devices, and steady progress has been made in the last 2-3 years. We anticipate that useful high K dielectric will be available for 65nm technology node and below.

High K dielectric for DRAM capacitor

DRAM capacitor must have a minimum capacitance of ~ 30 fF per cell in order to provide enough sensing margin and data retention time. When devices scale, the area occupied by the capacitor must scale in order to obtain a small cell size even when the capacitance stays fixed. For trench capacitor, the capacitor surface area must be increased by etching deeper trenches. For stacked capacitor, it is difficult to increase the surface area indefinitely and high K dielectric must be used to obtain smaller cell sizes.

To achieve high capacitance, the equivalent oxide thickness must be 1nm or lower. Unlike gate dielectric, the DRAM capacitor is very sensitive to leakage. The data retention time suffers greatly if the capacitor leakage exceeds ~ 1 fA/cell. The most commonly selected high K dielectrics are Ta_2O_5, Al_2O_3, or BST (Ba-Sr-Titanate) in order to ensure low leakage. These high K dielectrics also contain fixed charges that manifest into displacement current that degrades the access speed.

High K dielectric capacitors may be constructed using either polysilicon electrodes or metal electrodes. Polysilicon electrode has the advantage of simpler processing, but the disadvantage of high resistance which adversely impact the access speed of DRAM. Metal electrode, on the other hand, has low resistance but may interact strongly with both high K material and Si. Consequently, expensive noble metal such as Ir and Ru are used [2]. Metal oxides (high K) are extremely sensitive to plasma and hydrogen damage and thus need to be either protected or isolated from hydrogen and plasma. Recently, IrO_2 and RuO_2 electrodes are adopted because of their stabilizing effects on high K dielectric.

The successful application of high K dielectric will be the key to future high speed DRAM technology.

High K ferroelectrics for FeRAM capacitor

Most ferroelectrics have very high permittivity in the order of 500 – 1000. These dielectrics contain permanent dipoles that can be oriented by applying an electric field, and thus are suitable for non-volatile data storage. The memory cell is very similar to DRAM, consisted of a capacitor and an access MOS transistor. The storage node is usually in the form of a ferroelectric capacitor, with PZT ($Pb(Ti,Zr)O_3$) or SBT ($SrBi_2Ta_2O_9$) as the dielectric.

FeRAM not only is non-volatile, but also consumes little power during switching because it is a voltage device and not a current device. The datum is stored in the form of dipole polarization and thus requires no current to charge and discharge the capacitor. It is also very fast (< 100 ns access time) compared to other non-volatile memories for the same reason. Consequently, it becomes an ideal memory for embedded and SoC (System-on-Chip) applications – the most important being hand-held devices such as cellular phone, and contactless smart card which requires both high speed and low power.

High K ferroelectrics for FeRAM, however, face several daunting challenges. Both PZT and SBT require high temperature (650C – 700C) to form ferroelectric phase and even when noble metal electrode (Pt, Ru, Ir) is used it interacts with the ferroelectric. They also are extremely sensitive to plasma and hydrogen induced damage. In addition, oxygen vacancy at electrode interface causes severe fatigue degradation.

Recent progress in using IrO_2 electrodes has greatly alleviated the above problems and large array up to 32 Mb is demonstrated [3]. In addition, epitaxial growth of PZT on $LaNiO_3$ electrode at < 400C further allows the embedding of FeRAM in SoC using capacitor over interconnect (COI) modular concept [4].

References:

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