PATHWAYS FOR ADVANCED TRANSISTORS USING HAFNIUM – BASED OXIDES BY ATOMIC LAYER DEPOSITION

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The main challenge facing the gate stack community today is the continuous scaling of high-performance devices (target: EOT ≤ 1 nm, Jg ≤ 1 A/cm^2 and mobility approaching that of SiO_2), where there are no known solutions [1]. The focus is on Hf -based materials, including silicates, aluminates, and quaternary alloys, such as Hf-Si-O-N, and Hf-Al-O-N where the goal is to demonstrate an acceptable trade-off between dielectric constant and thermal stability. Additionally, the interface to Si needs to be carefully optimized to simultaneously achieve high mobility and low EOT values.

Atomic layer deposition (ALD) has generated a lot of interest for the growth of the high k-oxide due to the many benefits inherently offered by this technology [2]. There is an increasing number of publications showing leading edge work in the gate area using ALD to deposit Hf -based oxides and laminates [3-5]. At Genus, ALD was developed on a commercially established *LYNX 2* platform and subsequently scaled to 300 mm wafers on *LYNX 3*. Flexibility built into the hardware and software allows the engineering of interfaces and complex alloy and nanolaminate structures with high precision, reliability, and competitive throughput. Using the variation of thickness deposition rate per cycle as a metric, the variance with respect to process temperature, process pressure, pulse timings and purge timings have indicated an overall control capability on the order or less than 1% for Al_2O_3 and HfO_2 [6]. This process control is confirmed by the excellent leakage distributions reported in this presentation. Additionally, good composition control for the hafnium aluminates is established. Good trade-off between thermal stability and dielectric constant can be realized for 30 – 50 mol. % Al_2O_3, with favorable band offset values for low leakage [6, 7].

This presentation will review our current results on integration of ALD deposited Hf-based oxides in advanced transistors. As the interface between the Si and the high-k dielectric is of foremost importance for device performance, methods for surface treatment prior to the oxide deposition will be addressed. For example, the probability distribution of gate leakage in NMOS devices fabricated from 30 and 40 Å thick ALD HfO_2 layers with NH_3 and O_3 – based pre-treatment are shown in Figures 1 and 2, respectively. Both pre-treatments were carried out ex-situ. The results from SiO_2 – based devices are included for reference in both figures. Tight leakage distribution in the HfO_2 transistors is evidenced in both cases and the NH_3 – based pre-treatment yielded slightly lower leakage. Excellent Idsat and g_m with large overdrive were measured on these devices.

Additionally, the impact of the post deposition anneal (PDA) on leakage, EOT and mobility will be reviewed. Special attention is given to the trade-off between EOT and mobility presented by PDAs with and without oxygen containing ambient gases. Results from PMOS and NMOS devices will be compared and discussed with respect to integration differences and potential impact of B penetration.

References:

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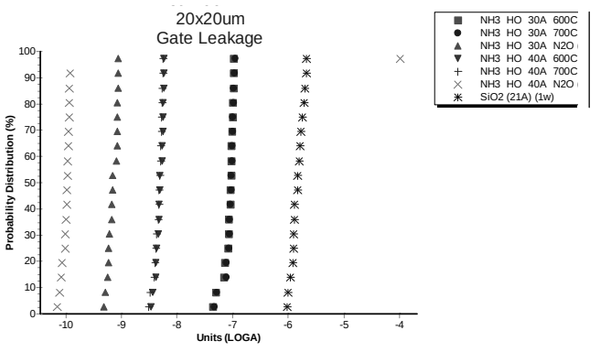

Figure 1 Probability distribution of gate leakage in NMOS devices fabricated from 30 and 40 Å thick ALD HfO_2 layers with NH_3 – based pre-treatment.

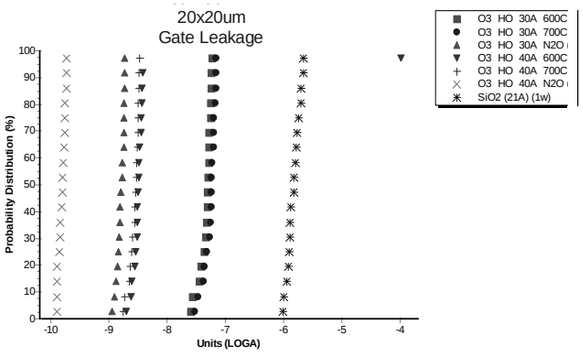

Figure 2 Probability distribution of gate leakage in NMOS devices fabricated from 30 and 40 Å thick ALD HfO_2 layers with O_3 – based pre-treatment.