Development of 12 Å Plasma Nitrided Gate Dielectrics through Correlation of Process, Physical, and Electrical Parameters

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Nitrided oxides have enabled scaling of advanced CMOS devices with gate dielectrics below 2nm. Nitridation reduces gate leakage and blocks boron penetration through the dielectric. Plasma nitridation has been shown to be a viable means of incorporating high levels of nitrogen that enable scaling. Correlation of plasma process, dielectric physical, and device electrical characterizations has enabled optimal scaling of the gate dielectric to below the 12 Å effective oxide thickness (EOT) required for high performance CMOS devices at the sub-90nm technology node.

Langmuir Probe (LP) and High-Resolution Optical Emission Spectroscopy (HR-OES) were used to characterize nitrogen plasmas in an Applied Materials' Decoupled Plasma Nitridation (DPN) chamber as a function of gas mixture, pressure, RF power, and RF pulse mode. Results are correlated with dielectric physical characterization by Photoemision Spectroscopy (PES) to determine nitridation rate and species.

Use of high-resolution surface techniques, such as PES, to characterize gate dielectrics is now possible. The gate dielectric thickness is now in a range where surface analysis techniques such as PES can be used to understand correlations between process conditions and near-interface bonding structure. The paper will explore ways in which these correlations may be helpful to better understand device electrical response for nitrided oxides.

Electrical device performance metrics such as drive current, gate leakage, and threshold voltage shift are correlated to plasma and dielectric parameters.

Single-wafer plasma nitridation also enables clustering of gate formation steps with low thermal budget. Clustering benefits have been demonstrated to enable further dielectric scaling with controlled interfaces.