Rapid Thermal Annealing of Hf-silicate/Polysilicon Dielectric Layers Deposited by Atomic Layer Deposition

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This work investigates the impact of rapid thermal processing on the physical and electrical properties of Hf-silicate (HSO) dielectric layers deposited by atomic layer chemical vapour deposition (ALCVD™). As gatelengths of MOSFETs are scaled down to 65nm and below, the gate control over the channel charge is reduced by short channel effects (SCE) and leakage currents become unacceptable high. To improve the gate control, a high-k gate stack that can withstand dopant activation anneals in the range 900-1100°C is required. HSO layers may fulfill some of the requirements, because they combine a relatively high crystallization temperature with acceptable k-value [1,2]. HSO layers were deposited using $HfCl_4$ and $NH_2(CH_2)_3Si(OC_2H_5)_3$ (APTES) as precursors. The composition and phase segregation in these layers was determined by Rutherford Backscattering (RBS) and X-ray Photoelectron Spectroscopy (XPS). Figure 1 shows RBS measurements of Hf-rich HSO layers after RTP. Clearly, the Hf is re-distributed after anneals above 600°C. The estimated Hf/(Hf+Si) ratio is 0.56 and 0.4 for $HfCl_4$:APTES ratios of 5:1 and 1:1, respectively. MOS capacitors with HSO dielectric layers and polysilicon electrodes were fabricated using various substrate preparations (O_3 start pulse, H_2O start pulse or ~1nm Al_2O_3). A HR-TEM study was performed to investigate the growth of interface layers and the stability of the HSO/polysilicon interface. Figure 2 shows TEM pictures of 48Å HSO, revealing growth of interface layers both at the Si-HSO and at the HSO-poly interface after 1000°C anneal. Capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements show that Si-rich (k~6) layers are not degraded up to 1000°C (Figure 3), 1s, but 1-2 orders leakage increase is above 900°C for Hf-rich (k~12) HSO layers (Figure 4). The observed effect is independent of the growth conditions. It is concluded that short time annealing is essential to suppress phase segregation and interface layer growth in HSO dielectric layers.

[1] A. Callegari *et al.*, J. Appl. Phys. **90**, 6466 (2001)
[2] B.C. Hendrix *et al.*, Appl. Phys. Lett. **80**, 2362 (2002)

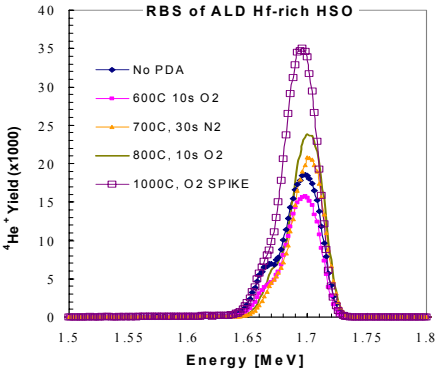

Figure 1. RBS measurements of Hf-rich HSO layers as function of RTP temperature.

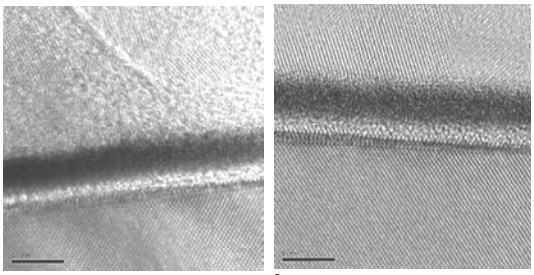

Figure 2. HR-TEM of ~48Å Hf-rich HSO dielectric layers with polysilicon electrodes. Left: as deposited. Right: after 1000°C, 1s RTP (5nm scale).

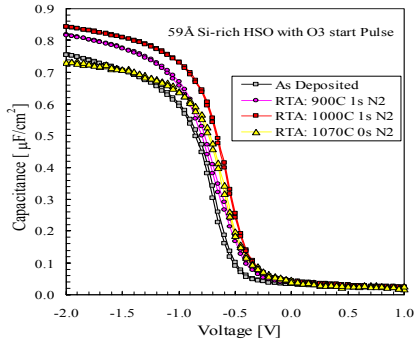

Figure 3. C-V of ~60Å Si-rich HSO as a function of RTP temperature.

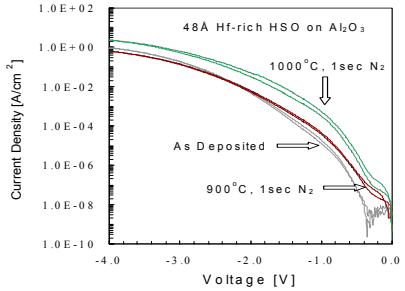

Figure 4. I-V measurements of 48Å Hf-rich HSO/poly after 900°C and 1000°C 1sec RTP.