High-κ Dielectric Processing for Ge-Channel MOSFETs

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The development of relatively high-quality deposited gate dielectrics to replace $SiO_2$-based dielectrics for silicon field effect transistors presents an opportunity to consider alternative materials for the semiconductor channel in such devices. There are many fundamental advantages to using Ge in the channel in place of Si. As shown in Fig.'s 1 and 2, fabrication of pMOSFETs on a Ge (100) channel is enabled by deposition of a $ZrO_2$ high-κ dielectric which is thermodynamically stable relative to $GeO_2$. The poor thermodynamic stability of $GeO_2$ may avoid growth of an undesirable low-κ oxide interface layer under the deposition conditions used to form the metal oxide high-κ gate dielectric, in contrast to the typical situation for high-κ deposition on Si. Furthermore, the greater dopant diffusivities in Ge appear to result in lower temperatures for dopant activation – source and drain activation can be achieved at $T \leq 400°C$. The smaller bandgap of Ge produces a smaller built-in junction potential. The larger (and better-matched) low-field carrier mobilities in Ge relative to Si result in devices that operate beyond the universal mobility model for Si MOSFETs.

In this presentation, results obtained from two different methods for controlled deposition of ultrathin metal oxides layers will be compared: atomic layer deposition (ALD) and UV-ozone oxidation (UVO). Physical characterization of $HfO_2$ and $ZrO_2$ gate dielectric layers and their interfaces with cleaned Ge (100) substrates will be emphasized. Electrical data obtained from MOSCAP structures and high-κ Ge MOSFETs will also be presented.

Deposition of a Zr metal processor film by PVD and its subsequent room temperature oxidation in the presence of UV light was found to produce an amorphous $ZrO_2$-containing dielectric layer on both DI water rinsed and HF-vapor treated Ge (100) surfaces.[1] This behavior stands in contrast to the observed structure of UVO-processed $ZrO_2$ films on $SiO_2$-passivated Si substrates, which have a polycrystalline tetragonal structure.[2] The resulting equivalent oxide thickness of the dielectric, derived from CV measurements of both high-κ/Ge MOSCAPs (Fig. 3) and pMOSFET devices is in the range 0.6 – 1.0 nm. Effective hole mobilities measured from long channel transistors with 3.5 nm thick $ZrO_2$-based gate dielectric layers[3] are approximately twice the values predicted from the Si MOSFET universal mobility model.[4]

In contrast, ALD growth of $ZrO_2$ onto similarly-prepared (100) Ge substrates from $ZrCl_4$ precursors at 300°C was found to produce an epitaxial gate dielectric. A <100> (100) $ZrO_2$//<100> (100) Ge orientation relationship was observed over a large area fraction of the dielectric film. However, the large (~ 10 %) lattice mismatch between the film and substrate resulted in the formation of a very high density of near-interface misfit dislocations. These defects may be responsible for the significant stretch out of the CV curves measured from shadow mask-defined Pt/ALD-$ZrO_2$/Ge MOSCAPs. Prospects for ALD growth of alternative metal oxides with closer lattice matching to Ge (100) will be discussed.

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3. S. Ramanthan, G.D. Wilk, D.A. Muller, C-M. Park, and P.C. McIntyre, Appl. Phys. Lett. **79**, 2621-23 (2001).
4. K. Chen, H. C. Wann, P. K. Ko, and C. Hu, IEEE Electron Device Lett. **17**, 202-04 (1996).

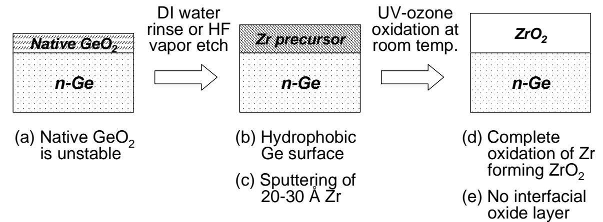


Figure 1. Illustration of the interlayer-free room temperature $ZrO_2$ deposition by the UV-assisted ozone oxidation of sputtered Zr precursor films.

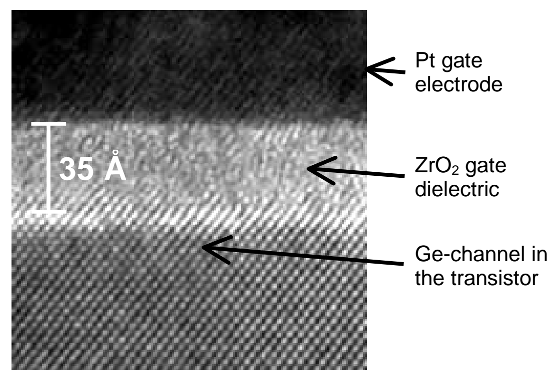


Figure 2. HR-TEM image taken from a fully processed Ge transistor.