Electrical Characterization of Thick Localized SOI Substrates Manufactured by Rapid Thermal Processing for High Voltage Integrated Circuits

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State of the art:

An important issue for power integration is the realization of high and low power devices in the same substrate, at low cost and with an efficient electrical insulation. Solutions to achieve the integration of many functions in the same chip or in the same substrate are the so-called BCD (Bipolar CMOS DMOS) technologies. While these solutions answer miniaturization needs, many issues cannot be solved using these techniques. Otherwise new materials like Silicon On Insulator (SOI) materials, commonly used for VLSI circuits, are now considered for high power specifications. For high voltage smart power applications, partial SOI substrates are more appropriate since the power device (either bipolar or MOS) is generally vertical and needs to be implemented on the bulk substrate, whereas the low voltage circuitry is dielectrically isolated (Fig.1). The fabrication of such a structure has to be cost effective and has to be part of the High Voltage Integrated Circuits (HVIC) process, while the existing SOI techniques are expensive and crystal quality and yield have still to be improved. Moreover, SOI wafers with local oxide layers are not commercially available.

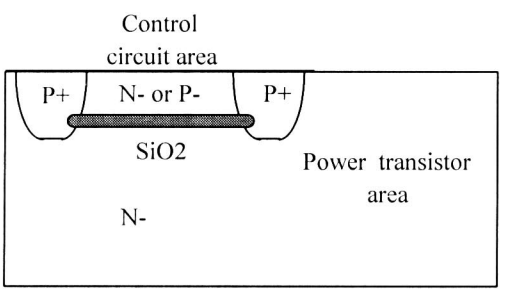

Figure 1: a typical smart power structure. The localized SOI region is vertically insulated from the bulk silicon by the SiO2 buried layer and laterally by junction isolation.

Purpose of the work and description of method:

We present a method for recrystallization of thick polysilicon films on top of SiO_2 layers by melting and solidification. This method, called Lateral Epitaxial Growth over Oxide (LEGO) uses a classical Rapid Thermal Processor (RTP) and while similar to Zone Melting Recristallization (ZMR), it avoids dangerous horizontal thermal gradient in the solid phase and therefore produces less defects, therefore allowing the formation of much thicker films than in any other melt-based technique. Indeed, regarding High Voltage Integrated Circuits (HVIC) application, the thickness of the silicon film on top of the buried oxide must be at least 10 µm. On the other hand, SiO_2 film thickness is not critical from a circuit point of view, however it has to be sufficient to thermally insulate the melted silicon film during the recrystallization step. Consequently, the oxide thickness must be at least 1 µm.

LEGO has been previously presented [1], and it has been already demonstrated that a single crystal silicon can be obtained over an oxide patterned layer (Fig.2). Thus fully recrystallized SOI islands of unlimited length and 500 µm width for a 10 µm epi-layer are available.

This paper concentrates on electrical performances of MOS transistors recently fabricated in the recrystallized areas.

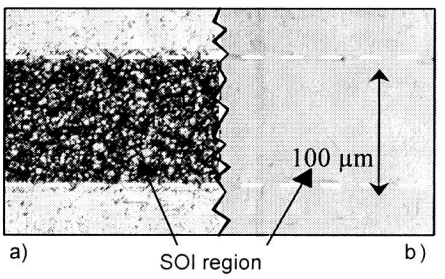

Figure 2: Top views (after Schimmel etch) of an SOI structure a) as deposited and b) after annealing. White dotted lines have been added to show the edges of the SOI area.

Results:

A test chip, including various dimensions and layouts for the SOI regions, together with PMOS devices, was designed to evaluate the physical and electrical properties of these layers. Crystalline quality of recrystallized layers was assessed via defect chemical revelation and TEM. analysis. It showed no extended defects [2]. The test chip included PMOS devices with several widths and orientations as well as different positions (edge and center) over the SOI regions. Witness wafers on bulk N- substrate underwent the same process than the SOI substrates.

The main results are as follows. First, PMOS electrical characteristics did not show any sensitivity to orientation with respect to the 4" wafer flat. In addition, the current of transistors with different widths properly scales with geometry. We made statistical electrical measurements, over a SOI (LEGO) wafer and a witness wafer, of two critical parameters for MOS transistors : channel mobility and subthreshold slope. Mobility is hardly affected by ~~this~~ LEGO process : transistors from witness wafer exhibits a mobility of 420 $cm^2/V.s$ whereas those from LEGO wafer presented the same mobilities, i.e. 376 $cm^2/V.s$ over SOI and bulk regions. Subthreshold slope is in the same range and has the same distribution for LEGO and witness wafers (Fig.3). This means that the observed fluctuations are not related to the LEGO process step but to the rest of the process. In the final paper, statistical wafer measurements will be presented.

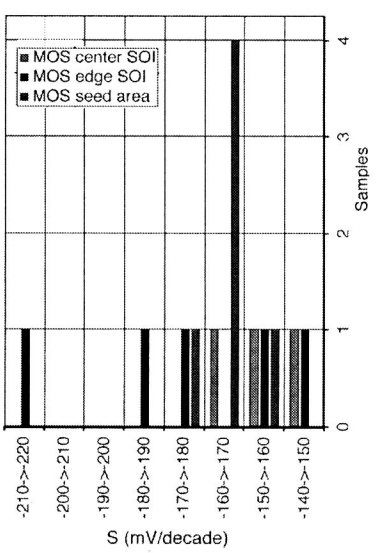

Figure 3 : Subthreshold slope of PMOS transistors realized on SOI and seed areas.

Conclusion and perspectives

The first electrical results obtained on recrystallized layers on SOI shows that characteristics of PMOS transistors keep very close to those of a witness wafer. In this test vehicle, the quality of the isolation was not evaluated. A new test chip is currently designed. It will implement both the full isolation scheme and high voltage power devices.

REFERENCES

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