# Design of Experiment on the Co Salicide Process : Impact of Thickness and Anneals on Main CMOS Parameters

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Use of Design of Experiment (DOE) is a very effective way to study a complex phenomenon with limited cost. Hence, a full modelisation by a polynom of 2nd order has been performed with only 21 wafers on the following cobalt salicide process (see also table I):

- Cobalt deposited by PVD
- 1st RTP anneal which transforms Co into CoSi
- Selective etch which removes unreacted Co
- 2nd RTP anneal which transforms the CoSi phase into $CoSi_2$, a less resistive phase.

This DOE allows concluding on the impact of process conditions on main CMOS parameters and helps to find the best trade-off for a complete integration into a 0.12µm CMOS process.

In particular, it is possible to show that the final $CoSi_2$ thickness is not only dependent on the Co thickness but also on the 1st RTP temperature (figure 1). This can be explained by an incomplete CoSi formation at low temperature : the unreacted Co is later removed during selective etch. This can be very useful when very low $CoSi_2$ thicknesses are desired and the control of PVD deposition reaches its limits.

The impact of the full process on active and poly resistance is also easily modelised. As expected, lower resistances are obtained with thicker Co layer. It is also possible to predict the minimum temperature and time necessary to obtain a full CoSi transformation. More interesting, is the clear evidence that 2nd RTP temperature has a major impact on resistance : hence, whatever the thickness, temperatures lower than 750°C do not lead to the optimum resistance (see figure 2).

The leakage mechanism of the N+/Pwell diode is also investigated. Co thickness, and 2nd RTP temperature are the major contributors to leakage current. It has been suggested that 1st RTP has also a strong impact on diode leakage [1] by changing the $CoSi_2$/Si interface. In our integration scheme, considering the fact that 1st RTP is impacting the final $CoSi_2$ thickness and that the leakage depends mainly on $CoSi_2$ thickness, 1st RTP temperature effect is of second order, compared to others parameters. On the opposite, increasing 2nd RTP anneal above 750°C allows a very strong reduction of the leakage current (see figure 3). This leakage reduction can not be explained by a dopant diffusion during the salicide process, as no change of the junction capacitance nor the active resistance is observed. This decrease is therefore consistent with the hypothesis made of $CoSi_x$ spikes defects at the $CoSi_2$/Si interface that would be restored by high temperature anneal [2].

Finally, it is also possible to observe the impact of the 2nd RTP on the deactivation of gate dopant. An increase of temperature from 700° to 850°C leads to a poly resistance increase of 4%. This is also associated with a gate depletion increase of 3.8Å to 4.4 Å but with negligible impact on global $I_{on}$ MOS performance. Nevertheless, this suggests that for sub 0.1µm technology nodes, the gate deactivation induced by the salicidation process could become a problem.

## REFERENCES

[1] T.S. Kang et al., Appl.Phys.Letter, 25 feb. 2002, vol 80, pp 1361-1363
[2] K. Goto et al., IEEE Trans. Electron Devices, January 1999, vol 46, No 1, pp 117-123

## FIGURES

| Parameters | Min | Max |
|---|---|---|
| Co Thick. | 60Å | 100Å |
| 1st RTP T°C | 430°C | 600°C |
| 1st RTP time | 0 sec | 60 sec |
| 2nd RTP T°C | 650°C | 850°C |
| Fixed RTP2 time | 20 sec | |

*Table I* : Experimental domain of the DOE

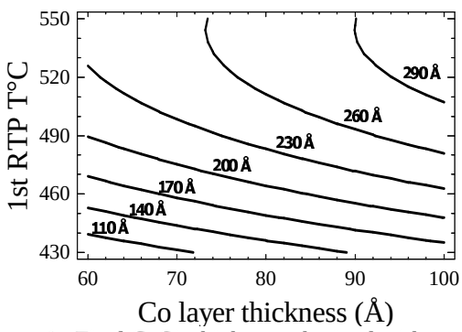


*Figure 1* : Final $CoSi_2$ thickness obtained with various RTP temperature or Co layer thicknesses.

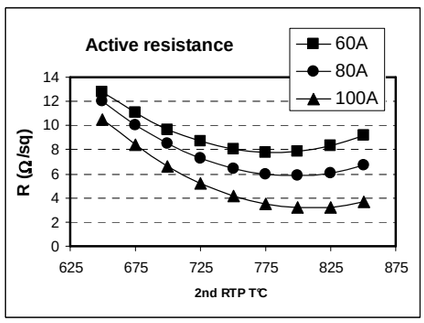


*Figure 2* : Variation of the salicided active resistance with 2nd RTP anneal, as modelised by the DOE.

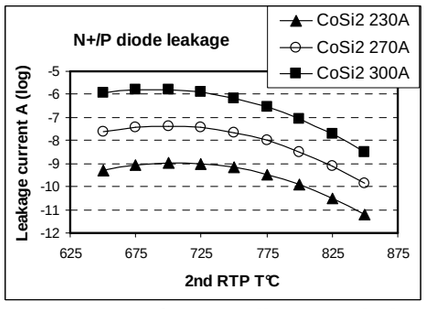


*Figure 3 :* Variation of N+/P well junction leakage with 2nd RTP temperature for various $CoSi_2$ final thickness.