Ultrathin Plasma Nitrided Oxide Gate Dielectrics for sub 100nm Generation CMOS Technology

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Recently, nitrided gate dielectrics are widely investigated to replace conventional dielectrics and to explore downscaling limits of gate dielectrics for the near future CMOS devices. In fact, several technologies for nitridation were proposed with results showing good electrical properties including low leakage currents and downscaled equivalent oxide thickness. However, other electrical properties such as Vt shift and mobility degradation related to the incorporation of high levels of nitrogen were observed. In this work, for further undestanding of plasma nitridation, fundamental properties of ultrathin nitrided gate dielectrics processed with DPN (decoupled plasma nitridation) were discussed. DPN was applied to ultrathin base oxides with continuous wave mode with plasma power in the range of 100W to 500W followed by post-annealing. For the evaluation of nitridation plasma, the effect of nitridation parameters such as plasma power, pressure, and time were analyzed in terms of N concentration, N bonding, and electrical properties including Tox,inv (Inv Tox, capacitance equivalent thickness measured in inversion region of CV).

The effect of plasma pressure on N concentration, optical and Quantox Tox was shown in Fig. 1. It may be seen from these figures, plasma pressure in the range of 5 to 80 mtorr significantly affected optical thickness and N concentration. The linear relation between optical thickness and N concentration was found for 11.3Å thick base oxide layers. Similar relations were also found with change of plasma time and power. It means N concentration adjusted by pressure can be easily estimated by the measurement of optical thickness, which is an important parameter affecting leakage current reduction and reliability. Leakage current density versus Inv Tox for NMOS processed at different plasma power is shown in Fig. 2. Also, the effect of post-annealing in N_2 or O_2 on Inv Tox or leakage current is shown in this figure. XPS analysis showed post-annealing in N_2 or O_2 after DPN interestingly induces more Si-N bond formation in nitrided layer from N-O bonds. High plasma power (300W) reduced leakage current by 8 times as compared to high quality control devices. The amount of leakage current improvement was affected by plasma power. It may be seen from this figure that post-annealing affects Inv Tox and leakage current. N_2 post-annealed devices showed lower Inv Tox by 1 to 2Å as compared to O_2 post-annealed devices. However, with 500W, thicker Inv Tox was measured. It may be due to the reoxidation of Si-Si bonds at interface by oxygen atoms generated during excessive nitridation of Si-O bonds to Si-N bonds. With N_2 post-annealing, Inv Tox can be scaled down more to 20.5Å. Fig. 3 shows Vt shift by plasma nitridation for NMOS and PMOS. In the case of PMOS, Vt shift increased upto 260mV from control devices. Vt shift was dependent on plasma power affecting N concentration, and NMOS showed much lower Vt shift as compared to PMOS. The larger PMOS Vt shift could be attributed to many nitrogen interaction such as boron penetration blocking, fixed charge, and nitrogen interacting oppositely with well dopants compared to NMOS devices. Fig. 4 shows comparative transconductance of reference and nitrided gate dielectrics post-annealed with N2. As shown in this figure, no transconductance degradation in nitrided dielectrics with plasma power of 100W or 200W was found. With higher plasma power (300W), mainly due to nitrogen induced Coulombic scattering, about 5% of transconductance degradation was measured as compared to reference oxide with 23Å Inv Tox without consideration of electrical thickness of dielectric layers. In this presentation, more fundamental properties analyzed by XTEM and XPS will be discussed.

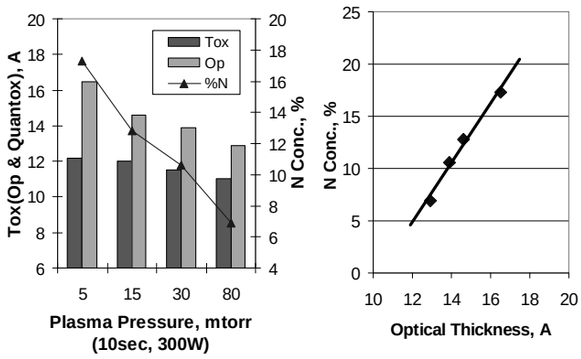

Fig.1, Effect of plasma pressure on Tox and N conc. (left) and relation between optical thickness and N conc. (right).

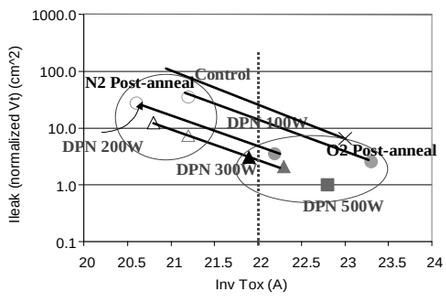

Fig. 2, Leakage current and Inv Tox.

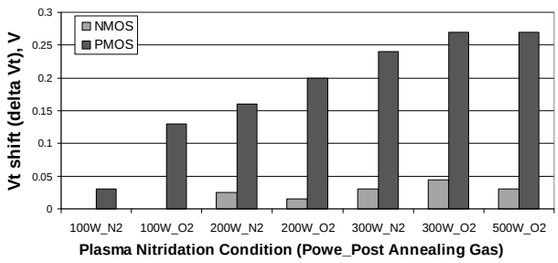

Fig. 3, Plasma power and Vt shift for NMOS and PMOS

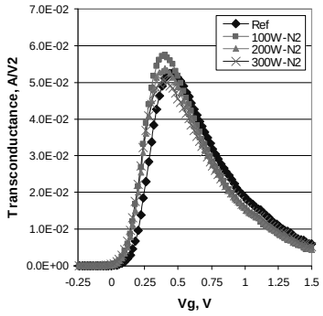

Fig. 4, Transconductance for reference and plasma nitrided gate dielectrics.