Silicon damage and dopant behaviour studies of rapid thermally processed ion implanted arsenic in silicon

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The search for new processes for shallow junction fabrication has led to focused development of new implantation techniques and rapid thermal processing, using incoherent tungsten-lamp irradiation, in order to provide ultra shallow junctions, with good electrical characteristics and good throughput at low cost for increasing wafer size. In this work, using low-energy implantation of As ions as well as the technique of rapid thermal annealing, RTA, very shallow n^+-p silicon junctions with a depth of ~60 nm have been fabricated and studied, reducing the diffusion of As atoms to a minimum, because of the short time of the annealing cycle. The implantation conditions were: energy 15keV and high dose $1x10^{15}cm^{-2}$ and the annealing conditions were: temperature 650ºC≤T≤950ºC (ramp-up rate of 70ºC/s) and time t=10 and 20 sec. A two-step annealing (650ºC/10s + 950ºC/10s) was performed in order to obtain shallower junctions. We used SIMS, sheet resistance methods and differential Hall effect measurements to study both the dopant diffusion and activation. SIMS measurements (Fig.1) show no As redistribution at 650ºC and only slightly broadened profiles at 750-850ºC. Profiles obviously broadened when the annealing temperature goes up to 950ºC by diffusion of As into the bulk and into the surface region. The sheet resistance decreases to173Ω/□ and the activation efficiency is about 60% at 950ºC/10s, whereas at 950ºC/20s a fraction of the dopant is lost from the surface resulting in the reduction in the active dose and therefore in an increase of about 33% in R_s. TEM study (Fig.2) revealed that at 650ºC/10s a defected zone with 9nm thickness is formed at a depth of 28nm, where the amorphous/crystalline Si interface was originally located and the crystallization of the amorphous layer is completed. Conventional and high-resolution TEM studies reveal that most defects are dislocation loops, although we were not able to exclude the existence of some precipitation. The dislocation loops have an average diameter of 4nm and are located almost parallel to the surface. By increasing the annealing temperature the thickness of the defected zone is increased, while simultaneously there is an increase of the mean diameter of the loops, which are transported closer to the surface, and finally at 950ºC/10s the loops are lost to the surface and the defected zone disappears.

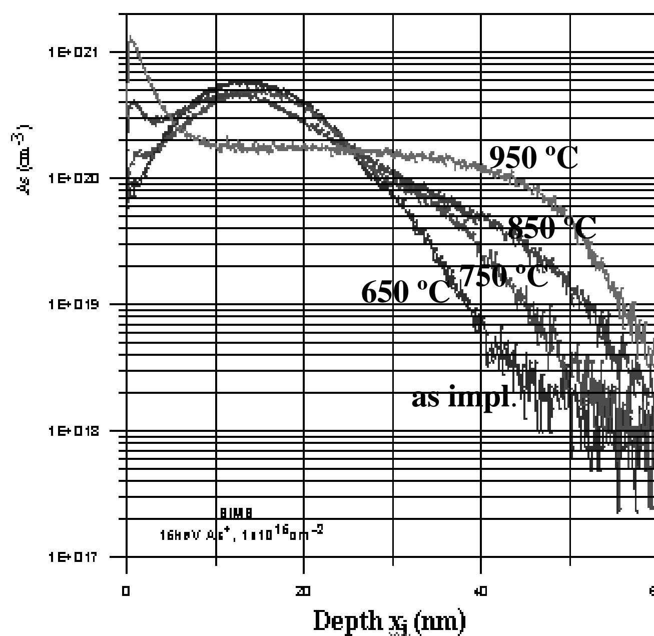

Fig. 1 SIMS depth profiles of As, as-implanted and annealed at different temperatures.

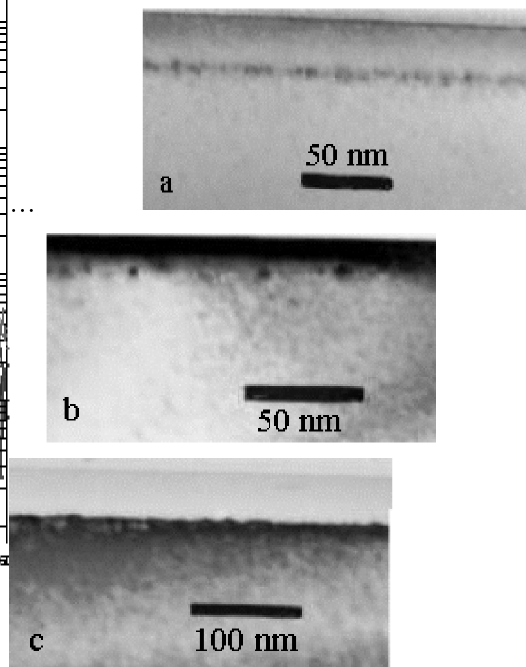

Fig. Fig. 2. TEM images for samples after RTA at a) 650ºC/10s, b) 750ºC /10s and c) 950ºC/10s.