ROADBLOCKS AND DETOURS FOR POLY-SILICON/METAL-OXIDE INTEGRATION

D. C. Gilmer, D. Triyoso, D. Roan, R. Cotton, J. Smith, R. Hegde, C. Hobbs, V. Dhandapani, R. Garcia, L. Dip, A. Franke, R. Rai, J. Grant, S. Samavedam, B. Taylor, H. Tseng, and P. Tobin

APRDL, DigitalDNA™ Laboratories, Motorola, Austin, TX 78721

Current technology forecasts show that continued deep sub-micron device scaling will soon require gate dielectrics to be thinned to much less than 1.5 nm EOT. To address this problem, high dielectric constant metal-oxide insulators are being extensively studied throughout the industry for use as gate dielectrics in ultra-scaled metal-oxide-semiconductor field-effect transistor (MOSFET) devices. However, incompatibilities with the desired MOSFET properties are observed with many of the dielectric systems presently under investigation. Here we report on results related to integration of various metal-oxide dielectric stacks, including hafnium-based systems, into poly-silicon gated MOSFETs and capacitors.

Metal-oxide gate-dielectrics used in ultra-scaled MOSFETs are desired to have properties that allow the use of conventional integration processes currently used with SiO_2 or Silicon-oxynitride gate-dielectrics. These properties would allow use of the current device architecture, CVD poly-crystalline silicon (poly-Si) gates, established dopant profiles, and thermal budget processing necessary for minimum poly-depletion. In addition, important device parameters like electrical thickness, dielectric leakage, threshold voltage and mobility of the fabricated devices need to be within an acceptable range for feasible application.

Typical gate-stack leakage current results using CVD Poly-Si gate on top HfO_2, SiO_2, and ALD-Al_2O_3 capped HfO_2 gate dielectrics are shown in Figure 1. Depositing Poly-silicon gates directly on HfO_2 results in films with high leakage. Even exposure of HfO_2 to SiH_4 at low temperatures can effect the electrical properties as shown in Figure 2. However, capping the HfO_2 with a monolayer of ALD-Al_2O_3 lowers the leakage by more than 10^4 compared to poly-Si on HfO_2 without the Al_2O_3 cap. Results for other stacks and capping layers (including hafnium-silicates, hafnium-aluminates, and lanthanum oxide systems), along with effects of varying the silicon-gate deposition temperature will also be reported. In addition to the high leakage seen for Poly-Si/HfO_2, large inhomogeneous grain growth (starlight) is often observed. These starlight defects are shown not to be the cause of the observed high leakage in Poly-Si/HfO_2. In the model to be presented here, the starlight defects are only a consequence of the same mechanism that is responsible for high leakage. We attribute the two observed effects to a partial reduction of the HfO_2 by the poly-Si deposition ambient. In the first case, the partial reduction occurs on the dielectric surface leading to starlight formation. In the second case, the poly deposition ambient (SiHx) diffuses into the bulk of the film along grain boundaries, where partial reduction occurs causing the high leakage. It is further concluded that any transition metal oxide is prone to adverse reaction from a SiHx ambient, the extent of which is dependent on the metal-oxide composition, surface defect distribution, energy of the metal-silicide formation, degree of metal-oxide crystallinity, and the poly deposition conditions.

Beyond obtaining compatibility with poly-Si gates for low leakage, is the need for acceptable threshold voltage and mobility. Normalized Gm values at 90% of SiO_2 controls were found for NMOS Poly-Si gate/Al_2O_3 capped HfO_2 (Fig. 3). Capacitance-voltage and mobility characteristics for various metal-oxide systems will be reported along with the effects of modulating the thermal budget of various processes.

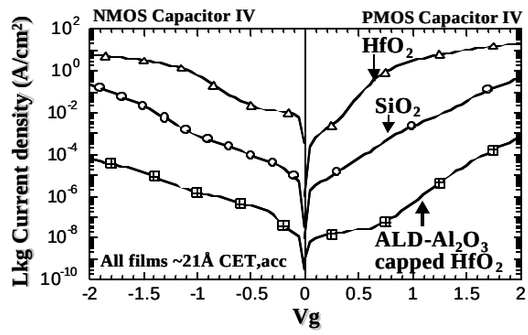

Fig. 1 I-V characteristics for HfO_2, SiO_2, and Al_2O_3-capped HfO_2 with Poly-Silicon gates.

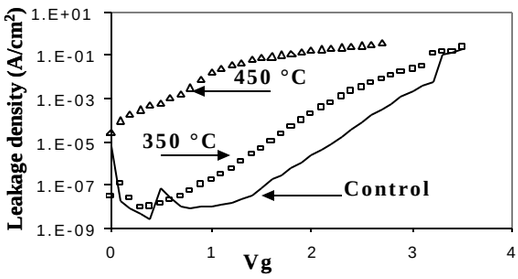

Fig. 2 Hg-probe leakage density for HfO_2 after exposure to SiH_4 at 350 °C or 450 °C compared to a control HfO_2 without SiH_4 exposure.

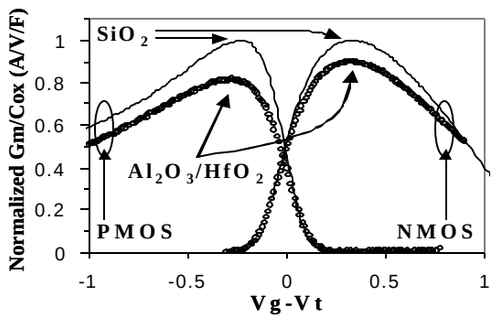

Fig. 3 Comparison of Gm normalized to the respective PMOS or NMOS Poly-Si gate/SiO_2 controls for Poly-Si gate/Al_2O_3 capped HfO_2 dielectric 25X25μm transistors.