Poly-Si Gate CMOS with Hafnium Silicate Gate Dielectric

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Silicon dioxide (SiO_2) has been the gate dielectric of choice because of its physical and electrical properties on silicon substrates. As MOSFET dimensions are scaled, the gate leakage current becomes unacceptably high when the SiO_2 is scaled to a thickness range where direct tunneling is the primary conduction mechanism. Recently, there has been much interest in hafnium based dielectrics as a potential high-k replacement for SiO_2 [1-4]. In this work, we have fabricated poly-Si gate $HfSi_XO_Y$ MOSFETs using a conventional 130nm CMOS process [1]. We will present results on the physical and electrical properties of devices with 20-40Å $HfSi_XO_Y$ with SiO_2 contents of 48-65%.

The $HfSi_XO_Y$ films were deposited by MOCVD. XPS analysis of unpatterened wafers was used to determine the composition. Cross-sectional TEM analysis showed that uniform films were produced. These blanket films remained amorphous at the MOSFET dopant activation temperature. Cross-sectional TEMs of a completed device are shown in Fig. 1.

Typical high frequency $HfSi_XO_Y$ CV curves for the 20Å films are shown in Fig. 2. Measurements taken from 0.1-1.0 MHz indicated no significant frequency dispersion. EOTs of 18.0 Å and 13.3 Å were extracted for the 20Å physical $HfSi_XO_Y$ with the 65% and 48% SiO_2 compositions, respectively. The gate leakage current decreases as the amount of Hf in the film is increased as shown in Fig. 3. In comparison to SiO_2, a gate leakage reduction of 28 X was obtained for $HfSi_XO_Y$ with the 13.3Å EOT.

The Id-Vg turn on behavior is shown in Fig 4. The subthreshold slope ranged from 80 to 89 mV/decade. For devices with similar CETinv, Fig. 5 indicates that a higher Hf content results in a lower transconductance. The threshold voltage roll-off shown in Fig. 6 shows that the $HfSi_XO_Y$ PMOS threshold voltage is higher than SiO_2 even when no channel implant is performed.

In summary, MOSFETs with $HfSi_XO_Y$ gate dielectrics were fabricated using a CMOS process. An EOT of 13.3 Å was achieved with a 28 X gate leakage reduction. Further work is needed to improve the high PMOS threshold voltages.

References

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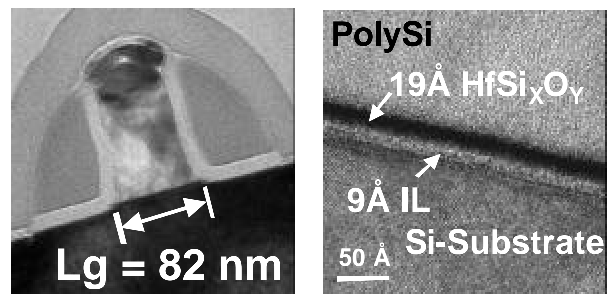

Fig. 1: Crossectional TEMs of a $HfSi_XO_Y$ MOSFET. The $HfSi_XO_Y$ composition is 65% SiO_2.

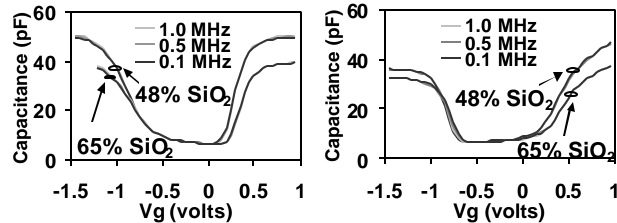

Fig. 2: Typical NMOS and PMOS CV curves for 20Å thick $HfSi_XO_Y$ with a 65% and 48% SiO_2 content.

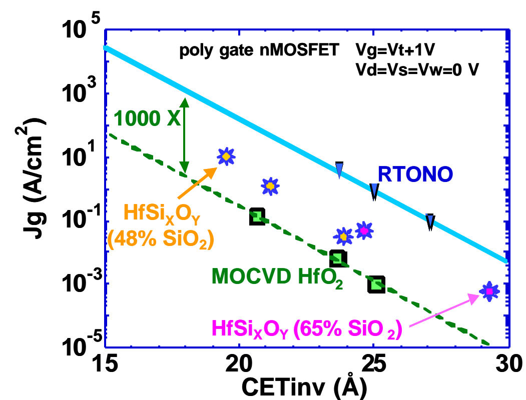

Fig. 3: Gate leakage current vs. CETinv.

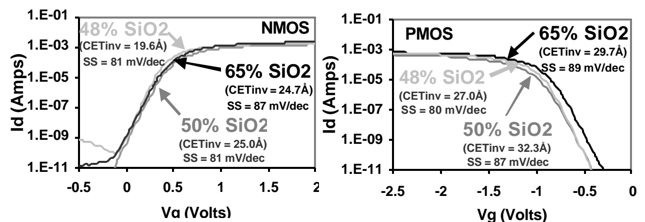

Fig. 4: Turn on Id-Vg characteristics for $HfSi_XO_Y$ with a 65% and 50% SiO_2 composition. (W/L = 10μm/80μm)

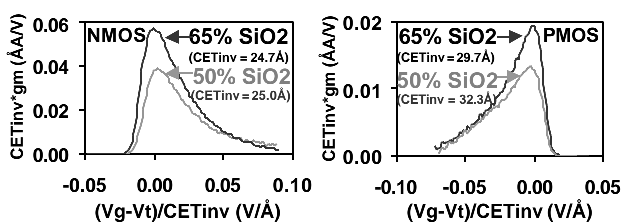

Fig. 5: Normalized peak gm for $HfSi_XO_Y$ with a 65% and 50% SiO_2 composition. (W/L = 10μm/80μm)

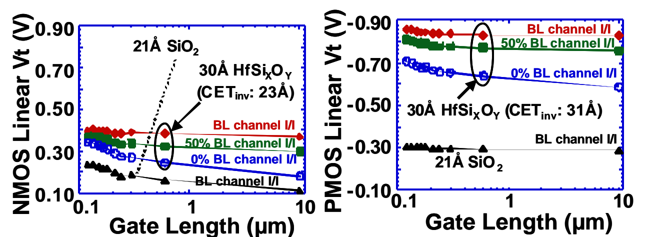

Fig. 6: MOSFET threshold voltage roll-off for SiO_2 and $HfSi_XO_Y$ with a 50% SiO_2 composition.