SELECTIVE OXIDATION OF TUNGSTEN-GATE STACKS IN HIGH VOLUME DRAM PRODUCTION

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Following the shrinkage of the critical dimensions of today's MOS FET, the conventional gate contact consisting of a stack of doped Polysilicon (p-Si) and Tungsten Silicide (WSi_x) is reaching its limits. With this combination of materials the required stack height to reach the target resistivities would lead to unacceptably high aspect ratios, which will result in difficulties in subsequent reactive ion etch (RIE) and fill steps. A solution could be the replacement of the WSi_x by a Tungsten / Tungsten Nitride (W/WN) stack. The specific resistances of W/WN allow low sheet resistivities in combination with small aspect ratios. In this stack the WN interface between p-Si and W acts as a barrier against silicidation during later thermal treatments.

After deposition and etching of the gate stack, state-of-the-art CMOS circuits receive a Rapid Thermal Oxidation (RTO). During this process the sidewall of the stack will be oxidized, and damage caused by RIE and implantation will be annealed, in order to decrease gate leakage and gate induced drain leakage. Due to the different oxidation behaviour of W/WN compared to WSi_x, the implementation of metal gate stacks requires the replacement of the non-selective RTO process by a selective oxidation. This selective process only oxidizes the lower p-Si sidewall while leaving the W/WN sidewall unoxidized.

Thermodynamical considerations as well as experimental data show a coexistence window of Si / SiO_2 and W for an ambient consisting of up to approx. 20% H_2O in H_2 at temperatures suitable for RT processing (800°C ... 1100°C) [1]

A selective process was developed on the Mattson 2800 Pyrogenic system, a tungsten-filament-lamp-based, double-side heated RTP system with pyrogenic steam generation in an external burner. The used material was 200 mm CZ grown <100> silicon wafers. The selectivity of this process was determined by ellipsometric thickness measurement of the SiO_2 layer, and four-point-probe measurement for sheet resistivity (R_S) of the p-Si/WN/W stack. The integrity of the WN barrier as a silicidation barrier was also shown with the R_S measurement.

However, the initial migration of the process toward high volume production showed process stability problems. Native Tungsten Oxides, especially Tungsten-Monoxide (WO), is volatile at elevated temperatures and evaporates from the sidewalls of the gate stacks. Condensation and partial reduction of the evaporates take place at the colder quartz tube walls disturbing the heat transfer by visible and infrared light. The demanded high temperature uniformity has required a cleaning of the RTP chamber every few wafers.

To overcome the problem of WO_x evaporation a four-parametric non-linear design of experiment (DOE) was carried out in order to determine the influences of the process parameters. The main interests are the process temperatures and the engineering of gas flows. In this experiment the WO_x outgasing has been determined by total reflection X-ray fluorescence analysis (TXRF).

The process with the lowest WO_x evaporation according to the DOE has been transferred to the Mattson 3000 Steam RTP system, located in an high volume DRAM production environment. Long term stability test has been carried out and the effect on the oxide thickness and uniformity has been monitored. More than 2000 wafers with planar W/WN layers were processed without changing or cleaning the quartz ware. Bare Silicon test wafers were run after every 25 W/WN coated wafers and showed no degradation of the oxide thickness or uniformity.

In summary, a selective sidewall oxidation process for the W/WN gate stack with good long-term stability was developed and released for production of advanced memory devices.

[1] T. Nagahama, N. Yamamoto, Y. Hanaoka, M. Saito, Y. Tanabe, 6th International Conference on Advanced Thermal Processing of Semiconductors, 1998, p.140 ff.

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