Performance of Nitrided Hf Silicate High k Gate Dielectrics

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As the devices are scaled down below 100nm aggressively, the equivalent oxide thickness of gate dielectrics based on SiO_2 or nitrided SiO_2 has been moved to direct tunneling region inducing high gate leakage current. To overcome this issue, high k gate dielectrics have attracted great attention for the next generation MOSFET devices. Among many candidate materials, Hf silicates were highlighted due to their thermally stable structure and better compatibility with poly-Si despite of the loss of dielectric constant advantage of Hf oxides. Most recently, nitrided Hf silicates by a reactive sputtering (PVD) technique using HfSi target were introduced with promising results [1]. In this paper, the performance of nitrided Hf silicates (HfSiON) prepared by a metal organic chemical-vapor-deposition technique (MOCVD) is discussed in terms of thermal stability, etchability, and electrical properties. In this work, after deposition, nitrided Hf silicate films were post-annealed with O_2/N_2. For the fabrication of transistors, conventional MOS process was used with poly-Si gate deposition. For comparison purposes, HfO_2 and Hf silicate (HfSiO) were deposited by a MOCVD technique, and 11.5Å and 17Å thick high quality oxides were also prepared. For the investigation of wet etch behavior, the removal rate of these films was measured as a function of time in dilute 100:1 HF solutions.

A cross-sectional TEM of MOCVD HfSiON layer under poly-Si after thermal annealing is shown in Fig. 1. Thin interfacial layer (≈6Å) was observed with smooth interfaces, and no interaction with poly Si was noticed. By XRD measurements, this layer was found to remain as an amorphous structure with thermal annealing at upto 1025°C in N_2. XPS showed a strong SiN bond peak indicating a large amount of nitrogen. It may suppress dopant penetration through high k layer. The etchability of nitrided Hf silicate was also studied in dilute HF. Wet etching properties of high k materials become critical because residual high k element on active area is not desirable before implantation and silicidation. Also, to prevent cross-contamination from the backside of high k wafers, wet etching properties should be investigated for back side wet cleaning. Fig. 2 shows the thickness changes of HfSiO and HfSiON as a function of HF dip time. Etching rate was found to be dependent on thermal history and materials. Lower temperature annealed wafers showed faster etching behavior, and HfSiON showed higher removal rate as compared to HfSiO. Hf silicates containing N were completely removed within a few minutes. Table 1 shows Quantox properties such as leakage resistance and Tox for HfSiO and HfSiON after annealing at 3 different temperatures. Interestingly, Dit and Vfb were affercetd by post-annealing, and Dit was decreased as the annealing temperature is increased. It was also found that as the annealing temperature in N_2 is increased, electrical thickness was increased. However, HfSiON showed lower thermal sensitivity (lower electrical thickness increase) indicating better thermal stability as compared to HfSiO. It may due to N acting as O diffusion barrier. Also, as shown in Table 1, for HfSiON, leakage resistance was increased (lower leakage current) as the electrical thickness was increased, while for HfSiO, leakage resistance was degraded as the electrical thickness was increased by thermal annealing. It should be noted that nitrided Hf silicates have excellent wet etching properties and barrier for interfacial layer growth by oxygen diffusion. Fig. 3 shows the gate leakage as a function of inversion Tox for HfSiON NMOS capacitors in comparison with SiO_2 control. For the same inversion Tox, leakage current was reduced by about two orders of magnitude with HfSiON. For the same gate leakage current, we gain ~5Å inversion Tox reduction with HfSiON. In this presentation, other electrical properties such as transconductance for HfSiON NMOS transistor with the SiO_2 control device will be presented.

References

[1] M. R. Visokay, et. al., Appl. Phys. Letter, 80 (17), 3183, 2002.

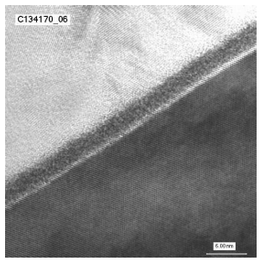

Fig. 1, Cross sectional TEM images of MOCVD HfSiON

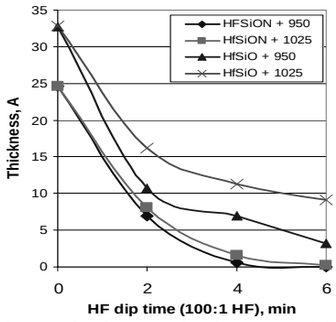

Fig. 2, Etching of HfSiO and HfSiON in dilute HF.

Table 1, Quantox properties of HfSiO and HfSiON.

Process Condition						
HfSiO	x	x	x			
HfSiON				x	x	x
Post Annealing						
N2 at 850C for 30s	x			x		
N2 at 950C for 30s		x			x	
N2 at 1025C for 30s			x			x
Dit (E12)	1.05	0.23	0.23	0.89	0.4	0.36
Leak (E16 ohm cm)	0.30	0.28	0.24	0.13	0.17	0.20
Tox (A)	10.6	13.1	14.7	9.5	11.1	11.8
Vfb (V)	0.05	0.22	0.39	0.20	0.30	0.33

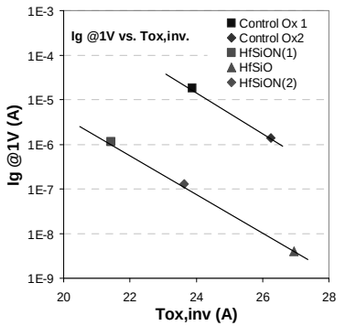

Fig. 3, Gate leakage current as a function of Tox,inv.